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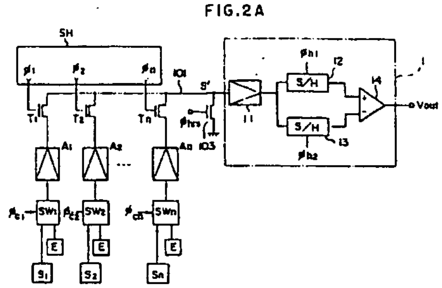
(54) **Solid state image pickup apparatus.**

(57) A solid state image pickup apparatus having a selector for selecting a plurality of sensor outputs through predetermined circuits includes a difference processing circuit for calculating a difference between a selected sensor signal and a reference signal selected through the same predetermined circuit as that of the selected sensor signal. The difference processing circuit includes a first holding circuit for holding the sensor signal, a second holding circuit for holding the selected reference signal, and a circuit for receiving the output signals from the first and second holding circuits and outputting a signal corresponding to a difference therebetween.

FIG.2A



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Description

Solid State Image Pickup Apparatus

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a solid state image pickup apparatus for selectively reading out a plurality of sensor signals and, more particularly, to a solid state image pickup apparatus capable of eliminating unnecessary components such as variations in dark signals and drive noise.

Related Background Art

Fig. IA is a schematic circuit diagram of a conventional solid-state image pickup apparatus.

Referring to Fig. IA, signals from sensors SI to Sn are respectively amplified by amplifiers AI and An, and transistors TI to Tn are sequentially turned on. A dot sequential output appears on an output line I0I. The dot sequential signal is amplified by a buffer amplifier I02, and the resultant signal appears as an output signal Vout.

In the conventional image pickup apparatus described above, variations in input/output characteristics of the amplifiers AI to An are included in the sensor signals as the dot sequential output appearing on the output line I0I. As a result, steady pattern noise undesirably occurs.

Fig. IB shows a schematic arrangement of another conventional photoelectric transducer apparatus.

Referring to Fig. IB, signals read out from photosensors SI to Sn are temporarily stored in storage capacitors CI to Cn. Transistors TI to Tn are sequentially turned on at timings of a scanning circuit SH, and the readout signals sequentially appear on an output line I0I and are output to an external device through an amplifier I02.

In the above photoelectric transducer apparatus, however, unnecessary components such as dark signals and drive noise of the photosensors are undesirably included.

Drive noise is defined as noise generated when a photosensor is driven to read out a signal. The drive noise components are noise caused by manufacture variations such as element shapes and smear caused by element isolation and depending on radiation amounts.

The dark signal is defined as a dark current of a photosensor and greatly depends on accumulation time and temperature of the photosensor.

This drive noise will be described in detail. Variations in drive capacity of a drive element for driving a photoelectric transducer element and variations in capacity of a photoelectric transducer element cause variations in leakage component of drive pulses. These variation components as an information signal are superposed on a necessary photoelectric transducer signal and are read out. The cause of generation of drive noise will be described below.

Fig. IC is a schematic view of a photoelectric transducer element described in Japanese Patent Laid-Open Gazette No. I2764/I985, Fig. ID is a timing chart of drive pulses for driving the photoelectric transducer element shown in Fig. IC, and Fig. IE is a chart showing the base potential of the photoelectric transducer element.

Referring to Fig. IC, the photoelectric transducer element includes a base accumulation type bipolar transistor B, a drive capacitor Cox for reverse- or forward-biasing the transistor B in response to a drive pulse φr, and a refresh transistor Qr. The transistor B has junction capacitances Cbc and Cbe. It should be noted that Cox, Cbc, and Cbe are referred to as capacitances or capacitors hereinafter, as needed. The capacitances Cox, Cbc, and Cbe are added to obtain a charge storage capacitance Ctot.

The operation of the photoelectric transducer element will be described below.

Assume that the initial value of a base potential VB is given as V0. When the drive pulse φr is set at a potential $V\varphi r$ at time tI, a voltage Va is applied to the base of the transistor B through the drive capacitor Cox. In this case, the voltage Va can be represented as follows:

$$Va = Cox/(Cox + Cbc + Cbe) \times V\varphi r = (Cox/Ctot) \times V\varphi r \quad \ldots (I)$$

When the drive pulse φrh is set at a high potential at time t2, a transistor Qr is turned on.

When the transistor B is forward-biased, the base potential VB is abruptly decreased. A time interval TC between time t2 and time t3 is a so-called refresh time interval.

The drive pulse φr is set at zero at time t3, and a voltage -Va is added to the base voltage VB, so that the base voltage VB is set at V2. This reverse-biased state is the accumulation state.

The above description was confined to one photoelectric transducer element. However, a line or area sensor has a large number of photoelectric transducer elements. The capacitances of the capacitors Cox, Cbc, and Cbe between a large number of photoelectric transducer elements vary by a few fractions of I%. For example, if the following conditions are given:

$$Cox = Cbc = Cbe \simeq 0.0I4\text{ pF, and } V\varphi r = 5\text{ V}$$

and the capacitance variation is 0.2 %, then a variation ΔVa in capacitance division voltage Va is about 3 mV.

The variation ΔVa can be reduced by refreshing. However, when the refresh mode is changed to an accumulation operation mode (time t3), the variation occurs again to produce ΔVb. The variation ΔVb does not satisfy relation $\Delta Vb = -\Delta Va$, and the correlation cannot be established therebetween according to test results.

The above fact is assumed to be derived from different bias voltage dependencies of Cbc anc Cbe.

In the next read cycle, when the transistor B is forward-biased, the variation in base potential thereof is approximated as follows:

$$\Delta V^2 \simeq \Delta Va^2 + \Delta Vb^2 + 2K\Delta Va\Delta b \quad \ldots (2)$$

for K is -l or more. As a result, the variation ΔV becomes steady drive noise of about 4 to 5 mV.

The variation in leakage component of such a drive pulse (to be referred to as drive noise hereinafter) is eliminated according to the following conventional technique. That is, the above drive noise is stored in a memory means and is read out and subtracted from the signal read out from the sensor to obtain a true information signal.

The conventional drive noise correction technique described above causes a bulky, expensive photoelectric transducer element which does not have any industrial advantage.

In particular, in case of that the numbers of elements arranged in the horizontal direction and vertical direction are five hundred respectively, an area sensor requires 250,000 photoelectric elements arranged in a matrix form. In addition, when the resolution of the sensor is also taken into consideration, a memory of several megabits is required.

The unnecessary signals such as drive noise and a dark signal pose serious problems when an image of a dark object is to be picked up, i.e., image pickup at a low intensity. In the low-intensity image pickup mode, an information signal level is low and accordingly the S/N ratio is degraded. As a result, image quality is degraded. In order to improve image quality, the unnecessary signals must be reduced.

As described above, however, the dark signal primarily depends on temperature and charge accumulation time, although the drive noise rarely depends thereon. If these unnecessary signals are to be eliminated, the dark signal must separated from the drive noise and a correction coefficient must be determined, thus requiring a large-capacity memory. As a result, signal processing is complicated and expensive, and an image pickup apparatus is undesirably bulky.

SUMMARY OF THE INVENTION

It is an object of the present invention to eliminate the conventional drawbacks described above.

It is another object of the present invention to eliminate variations in drive noise in units of sensor cells.

It is still another object of the present invention to compensate for variations in electrical characteristics of a plurality of amplifiers arranged for sensor cells.

In order to achieve the above objects according to an aspect of the present invention, there is provided a solid state image pickup apparatus having a selector for selecting a plurality of sensor signals through corresponding amplifiers, comprising a processing circuit for calculating a difference between a selected sensor signal and a reference signal selected through the same circuit for selecting the sensor signal.

The sensor signal selected by the selector, therefore, includes a noise component caused by variations in amplifier characteristics since the sensor signal is amplified by the corresponding amplifier. For this reason, the reference signal is selected through the same amplifier which has amplified the sensor signal, so that the amplifier noise is superposed on the reference signal. A difference between the selected sensor signal and the selected reference signal is calculated to eliminate the noise component.

According to another aspect of the present invention, there is provided a photoelectric transducer apparatus having storage means for storing a signal from a photoelectric transducer element, wherein the storage means comprises first storage means for storing the signal read out from the photoelectric transducer element and second storage means for storing a residual signal after the photoelectric transducer element is refreshed, and further comprising difference processing means for calculating a difference between the readout and residual signals respectively stored in the first and second storage means.

Since the residual signal obtained upon completion of refreshing is subtracted from the readout signal, the unnecessary components such as a dark signal and drive noise of the photoelectric transducer element can be eliminated.

A MOS, electrostatic induction, or base accumulation type photosensor may be used as a photoelectric transducer element.

"Refreshing" of the photoelectric transducer element means erasure of optical information of the photoelectric transducer element. In some photosensors, optical information is erased simultaneously when the information is read out. However, in some photosensors, optical information is kept unerased even after the information is read out.

According to still another aspect of the present invention, in order to eliminate the conventional drawbacks described above, there is provided a solid state image pickup apparatus comprising a plurality of photoelectric transducer elements, first storage means, arranged in units of photoelectric transducer elements, for storing a video signal, second storage means, arranged in units of photoelectric transducer elements, for storing noise components, first readout means for simultaneously and independently reading out signals for photoelectric transducer elements of a plurality of horizontal lines from the first storage means, and second readout means for adding signals for the photoelectric transducer elements of the plurality of horizontal lines from the second storage means and for reading out a sum signal.

With the above arrangement, it is assumed that the drive noise is generated as a sum of noise components generated in the refresh, charge accumulation, and readout modes of the photoelectric transducer element and the drive noise level is substantially identical in each mode. A difference between the photoelectric transducer signal read out upon completion of exposure and drive noise read out in the photoelectric transducer signal readout mode is calculated to eliminate the drive noise. It should be noted that the noise components are read out after they are added, thereby reducing the number of read lines.

According to still another aspect of the present invention, in order to eliminate the conventional drawbacks described above, there is provided a

solid state image pickup apparatus comprising photoelectric transducer elements, a plurality of storage capacitors for storing readout signals when the photoelectric transducer elements are read-accessed a plurality of times, dot sequential processing means for converting signals from the storage capacitors into a dot sequential signal, and clamping means for clamping some components of the dot sequential signal from the dot sequential processing means.

With the above arrangement, it is assumed that the drive noise is generated as a sum of noise components generated in the refresh, charge accumulation, and readout modes of the photoelectric transducer element and the drive noise level is substantially identical in each mode. The photo electric transducer signal read out upon completion of exposure and drive noise read out in the photoelectric transducer signal readout mode are converted into a dot sequential signal, and the drive noise component is clamped, thereby eliminating the drive noise included in the photoelectric transducer signal components.

The above and other objects, features, and advantages of the present invention will be apparent from the following detailed description in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. IA is a schematic circuit diagram of a conventional solid state image pickup apparatus;

Fig. IB is a schematic view of another conventional solid state image pickup apparatus;

Figs. IC to IE are views for explaining the principle of generation of drive noise of a photoelectric transducer element;

Figs. 2A and 2B are schematic circuit diagrams showing a solid state image pickup apparatus according to an embodiment of the present invention;

Fig. 3 is a circuit diagram showing an arrangement of switches SWI to SWn in the apparatus of Fig. 2A;

Fig. 4 is a circuit diagram showing another arrangement of switches SWI to SWn in the apparatus of Fig. 2A;

Fig. 5A is a circuit diagram showing another arrangement of a difference processing circuit in the apparatus of Fig. 2A;

Fig. 5B is a timing chart for explaining the operation of the difference processing circuit shown in Fig. 5A;

Fig. 6A is a schematic circuit diagram showing a solid state image pickup apparatus according to another embodiment of the present invention;

Fig. 6B is a timing chart for explaining the operation of the apparatus shown in Fig. 6A;

Fig. 7 is a block diagram showing an image pickup system using the apparatus (of any embodiment described above) as an image pickup device;

Fig. 8A is a schematic sectional view of a photoelectric transducer cell described in Japanese Patent Laid-Open Gazettes Nos. I2759/I985 to I2765/I985.

Fig. 8B is an equivalent circuit diagram thereof;

Fig. 9 is a graph showing the relationship between a width $\underline{t}$ of a refresh pulse applied to the photoelectric transducer cell and a photoelectric transducer cell output after refreshing;

Fig. I0 is a circuit diagram for explaining a basic arrangement of a solid state image pickup apparatus according to still another embodiment of the present invention;

Fig. II is a timing chart for explaining the operation of the apparatus shown in Fig. I0;

Fig. I2 is a circuit diagram showing the overall arrangement of the apparatus shown in Fig. I0;

Figs. I3A and I3B are timing charts for explaining two operation modes of the apparatus shown in Fig. I0;

Fig. I4 is a circuit diagram of a solid state image pickup apparatus according to still another embodiment of the present invention;

Fig. I5 is a detailed circuit diagram of a readout circuit Ri in the apparatus shown in Fig. I4;

Fig. I6 is a timing chart for explaining the operation of the apparatus shown in Fig. I4;

Fig. I7 is a block diagram showing an image pickup system using the apparatus (Fig. I0) as an image pickup device;

Fig. I8 is a circuit diagram showing an image pickup apparatus according to still another embodiment of the present invention;

Fig. I9 is a block diagram showing an image pickup system using the image pickup apparatus (Fig. I8) as an area sensor;

Fig. 20 is a circuit diagram of a solid state image pickup apparatus according to still another embodiment of the present invention;

Fig. 2I is a timing chart for explaining the operation of the apparatus shown in Fig. 20;

Fig. 22 is a schematic view showing an arrangement when the apparatus in Fig. 20 is applied to an area sensor; and

Fig. 23 is a timing chart for explaining the operation of the area sensor shown in Fig. 22.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described with reference to the accompanying drawings hereinafter.

Fig. 2A is a schematic circuit diagram of a solid state image pickup apparatus according to an embodiment of the present invention.

Referring to Fig. 2A, switches SWI to SWn are arranged to select corresponding inputs in response to pulses φcI to φcn. The switches SWI to SWn respectively receive sensor signals SI to Sn from photosensors SI to Sn arranged in a line or a matrix form. The switches SWI to SWn also receive signals E from reference signal sources E, respectively.

The output terminals of the switches SWI to SWn

are respectively connected to the input terminals of amplifiers AI to An. The output terminals of the amplifiers AI to An are connected to an output line I0I through corresponding transistors TI to Tn. Pulses φI to φn from a scanning circuit SH such as a shift register are respectively supplied to the gate electrodes of the transistors TI to Tn. The transistors TI to Tn are turned on in response to the pulses φI to φn.

The output line I0I is grounded through a transistor I03. A pulse φhrs is applied to the gate electrode of the transistor I03. The output line I0I is also connected to a difference processing circuit I. An output signal Vout free from noise components is output from the difference processing circuit I.

In the difference processing circuit I in this embodiment, the output line I0I is connected to an amplifier II. The input terminals of sample/hold (S/H) circuits I2 and I3 are connected to the output terminal of the amplifier II. Pulses φhI and φh2 as control signals are respectively supplied to the S/H circuits I2 and I3 so that the S/H circuits I2 and I3 hold the inputs at the input timings of these pulses, respectively. The output terminals of the S/H circuits I2 and I3 are respectively connected to the noninverting and inverting input terminals of a differential amplifier I4. The output signal Vout is output from the differential amplifier I4.

The operation of this embodiment will be described below.

When the reference E is input to the amplifier AI upon operation of the switch SWI, the reference signal E is amplified by the amplifier AI, and an amplified signal EI′ is output to the transistor TI. In this case, only the transistor TI is kept on in response to the pulse φI, and other transistors T2 to Tn are kept off. The reference signal EI′ is selected by the transistor TI and appears on the output line I0I. The reference signal EI′ is held in the S/H circuit I2 through the amplifier II. More specifically, the pulse φhI is supplied to the S/H circuit I2 when it holds the reference signal EI′.

The reference signal EI′ held by the S/H circuit I2 is a signal reflecting variation characteristics of the amplifier AI, i.e., a signal including a noise component NI which becomes a steady pattern noise. In other words, EI′ = E + NI.

Subsequently, the transistor I03 is turned on in response to the pulse φhrs to remove the charge left on the output line I0I. An output signal from the sensor SI is input to the amplifier AI through the switch SWI. In the same manner as described above, a sensor signal SI′ amplified by the amplifier AI appears on the output line I0I through the ON transistor TI and is held by the S/H circuit I3 through the amplifier II.

The sensor signal SI′ held by the S/H circuit I3 also reflects variation characteristics, i.e., a signal including the noise component NI (SI′ = SI + NI).

When the reference signal EI′ and the sensor signal SI′ are respectively held by the S/H circuits I2 and I3, the signals SI′ and EI′ are input to the differential amplifier I4. The output Vout from the differential amplifier I4 is a difference (SI′ - EI′) between the sensor and reference signals SI′ and EI′, thereby obtaining a signal (SI - E) free from the noise component NI. In this case, the reference signal E represents the reference level of the sensor signal SI, so that E = 0 is established. Therefore, the output signal Vout is the sensor signal SI before being subjected to the influence of the amplifier AI.

When the sensor signal SI is output in this manner, the residual charge on the output line I0I is eliminated by the transistor I03. At the timings in the same manner as described above, the sensor signals S2 to Sn free from the noise components N2 to Nn are sequentially output from the differential amplifier I4.

In the above description, the reference signal E is read out prior to the corresponding sensor signal. However, each sensor signal may be read out prior to the reference signal E.

In the above description, the reference and sensor signals EI′ and SI′ are held in the separate S/H circuits, respectively. However, one of the S/H circuits may be omitted, and the output terminal of the amplifier II may be directly connected to the amplifier I4 (Fig. 2B). In this case, one readout signal is held by the S/H circuit I2 in response to the pulse φhI, and the output signal Vout is output from the differential amplifier I4 at the read timing of the other readout signal.

Fig. 3 is a circuit diagram showing an arrangement of switches SWI to SWn in the apparatus shown in Fig. 2A.

Referring to Fig. 3, a transistor 20I is turned on in response to a pulse φt to store the sensor signal SI in a capacitor CI. Subsequently, a transistor 203 is turned on in response to a pulse φcb to output the reference signal E to the amplifier AI.

When the reference signal EI′ is held as described above, the transistor 202 is turned on in response to a pulse φca to output the sensor signal SI from the capacitor CI to the amplifier AI.

The switches SW2 to SWn have the same arrangement as that of the switch SWI, and operations of the switches SW2 to SWn are also the same as that of the switch SWI.

Fig. 4 is a circuit diagram showing another arrangement of the switches SWI to SWn in the apparatus of Fig. 2A.

In this arrangement, the reference signal E is generated by drive noise caused by variations in leakage component of the sensor.

Referring to Fig. 4, a transistor 30I is turned on in response to a pulse φtI to store the sensor signal SI in a capacitor CII. Subsequently, a transistor 303 is turned on in response to a pulse φt2. A sensor signal representing absence of optical information or the dark state thereof serves as the reference signal E. This reference signal E is stored in a capacitor CI2. In this state, a drive noise component of the corresponding sensor is stored in the capacitor CI2. In the same manner as described above, a transistor 304 is turned on to output the reference signal E from the capacitor CI2 to an amplifier AI and then a transistor 302 is turned on to output the sensor signal SI from the capacitor CII to the amplifier AI.

By using the sensor drive noise component as the reference signal E, the output Vout (= SI′ - EI′) from

the differential amplifier I4 is free from the sensor drive noise component as well as the noise component NI of the amplifier AI.

Fig. 5A is a circuit diagram showing another arrangement of the difference processing circuit in the apparatus shown in Fig. 2A, and Fig. 5B is a timing chart for explaining the operation thereof.

Difference processing is performed by a clamping circuit in this arrangement.

Referring to Figs. 5A and 5B, the reference signal EI′ amplified by the amplifier AI appears on the output line I0I and is input to a clamp circuit through an amplifier comprising transistors I5 and I6. In this case, the clamp circuit comprises a capacitor I7 and a transistor I8. Since the transistor I8 in the clamp circuit is kept on in response to a clamp pulse φs, the level of the reference signal EI′ is clamped as the reference level. As a result, the sensor signal SI′ subsequently appearing on the output line I0I is amplified by an amplifier of transistors I9 and 20 using the reference signal EI′ as a reference level. In the same manner as in Fig. I, the output signal Vout obtained by removing the reference signal EI′ from the sensor signal SI′ is obtained. Similarly, the clamp pulse φs is generated at a read timing of the reference signal EI′, and the sensor signals SI to Sn free from the noise components are sequentially output.

Fig. 6A is a schematic circuit diagram of a solid state image pickup apparatus according to another embodiment of the present invention, and Fig. 6B is a timing chart for explaining the operation thereof.

Referring to Fig. 6A, sensors BI to Bn (to be referred to as B hereinafter) are base accumulation type phototransistors. A base potential of each transistor is controlled through a capacitor, and the carriers excited upon incidence of light are accumulated in the base region of the transistor. The accumulated voltage is read out as a sensor signal, or the accumulated carriers are removed.

A read or refresh pulse φr is applied to the capacitor electrodes of the sensors B. The emitter electrodes of the sensors B which are adapted to read out sensor signals SI to Sn (to be referred to as S hereinafter) are grounded through transistors QrI to Qrn (to be referred to as Qr hereinafter), respectively. The emitter electrode are connected to temporary storage capacitors CII to CnI through transistors QaI to Qan (to be referred to as Qa hereinafter) and to temporary storage capacitors CI2 to Cn2 through transistors QcI to Qcn (to be referred to as Qc hereinafter), respectively.

The capacitors CII to CnI are connected to the gate electrodes of amplifiers AI to An through transistors QbI to Qbn, respectively. The capacitors CI2 to Cn2 are connected to the gate electrodes of the amplifiers AI to An through transistors QdI to Qdn, respectively.

A voltage Vcc is applied to the first terminals of the amplifiers AI to An, and an output line 50I is commonly connected to the second input terminals thereof.

A pulse φaI is applied to the gate electrodes of the transistors QbI to Qbn through transistors QeI to Qen. A pulse φbI is applied to the gate electrodes of the transistors QdI to Qdn through transistors QfI to Qfn.

Pulses φI to φn from a scanning circuit SH are sequentially supplied to the gate electrodes of the transistors QeI to Qen, QfI to Qfn, and TI to Tn, respectively.

A transistor 502 is connected to the output line 50I, and a voltage Vss is applied to the output line 50I through the transistor 502. A signal S′ amplified by each amplifier and appearing on the output line 50I is input to the difference processing circuit I, and difference processing as described above is performed. It should be noted that the difference processing circuit I in this embodiment is of a differential type using the S/H circuit shown in Fig. 2A.

The operation of the apparatus of this embodiment will be described with reference to Fig. 6B.

Assume that carriers corresponding to the intensity levels of the incident light are stored in the base regions of the sensors B, respectively.

For a time interval TmI, the transistors Qr are kept on in response to the pulse φrh, and the emitter electrodes of the sensors B and the vertical lines are grounded. At the same time, the transistors Qa and Qc are turned on in response to the pulses φtI and φt2 to clear the carriers from the capacitors CII to CnI and CI2 to Cn2, respectively.

For a time interval Tm2, the transistors Qa are kept on in response to the pulse φtI to supply the read pulse φr to the sensors B. Therefore, the sensor signals S from the sensors B are stored in the capacitors CII to CnI, respectively. These sensor signals include the drive noise components of the corresponding sensors.

For a time interval Tm3, the transistors Qr are kept on in response to the pulse φrh to ground the emitters of the sensors B. The sensors B are refreshed in response to the refresh pulse φr. Upon completion of refreshing, the transistors Qrh are turned off, and the transistors Qc are turned on in response to the pulse φt2. During this period, the read pulse φr is applied to read out the signals from the sensors B. Their drive noise components, i.e., the above-mentioned reference signals EI to En are respectively stored in the capacitors CI2 to Cn2 Thereafter, the pulse φr falls to cause the sensors B to start charge accumulation.

The above operations are performed during a blanking period BLK, and the signals temporarily stored in the corresponding capacitors are sequentially read out onto the output line 50I.

The transistors TI, QeI, and QfI are turned on in response to the pulse φI. The voltage Vcc is applied to the amplifier AI, and the amplifier AI is rendered operative (other amplifiers A2 to An are rendered inoperative). The pulse φaI rises in synchronism with the pulse φI and the transistor QbI is turned on through the ON transistor QeI. The sensor signal SI stored in the capacitor CII is amplified by the amplifier AI, and the amplified signal appears on the output line 50I and is then held in an S/H circuit I2 in a difference processing circuit I.

Subsequently, the pulse φbI rises and then the transistor QdI is turned on through the transistor QfI.

The reference signal El stored in the capacitor Cl2 is amplified by the amplifier Al, and the amplified signal appears on the output line 50l and then held by an S/H circuit l3.

It can be assumed that a potential of an input to the amplifier Al can be reset to a reference potential for a period from the time when the sensor signal Sl is output from the capacitor Cll to the amplifier Al and to the time when the reference signal El is output from the capacitor Cl2.

However, most of the input capacitance of the amplifier Al is an overlap capacitance of the transistors. The input capacitance is sufficiently smaller than the capacitances of the capacitors Cll and Cl2, and the residual charge can be neglected. Steady pattern noise caused by variations in amplifier characteristics is typical when the image signal is small. In this case, the residual charge is further decreased.

From the above reasons, a means for resetting the input terminals of the amplifiers Al to An is omitted. However, in an application wherein the residual charge cannot be neglected, a reset means must be connected to the inputs of the amplifiers A.

When the sensor and reference signals Sl' and El' are respectively held by the S/H circuits l2 and l3, the above-mentioned difference processing is performed to cause the differential amplifier l4 to produce the sensor signal Sl as the output signal Vout free from the drive noise component and the noise component Nl. Similarly, the sensor outputs Sl to Sn are sequentially output.

When all sensor signals are output, the next sensor signals corresponding to the incident light are stored in the sensors B. In the same manner as described above, sensor read access and refreshing are performed for the blanking period BLK. Charge accumulation of the sensors B and dot sequential operation of the sensor signals temporarily stored in the capacitors are simultaneously performed.

When the clamp circuit shown in Fig. 5 is used in the difference processing circuit l, the capacitor Cl2 for charging the reference signal El and then the capacitor Cll for charging the sensor signal Sl must be discharged. This applies to the signal readout operations of the sensor signals S2 to Sn.

Fig. 7 shows a schematic arrangement of an image pickup system using any one of the image pickup apparatuses of the embodiments as an image pickup device.

Referring to Fig. 7, an image pickup device 60l comprises an image pickup apparatus of any one of the above embodiments. The gain or the like of the output signal Vout is controlled by a signal processing circuit 602, and the resultant signal is output as a video signal.

Various pulses φ for driving the image pickup device 60l are supplied from a driver 603. The driver 603 is operated under the control of a control unit 604. The control unit 604 controls the gain or the like of the signal processing circuit 602 on the basis of the output from the image pickup device 60l and also controls an exposure control unit 605 to adjust an amount of light incident on the image pickup device 30l.

As described above, in the solid state image pickup apparatus according to the above embodiments, a difference between the selected sensor signal and the selected reference signal is calculated to obtain an output signal free from the noise components. Therefore, the variations in readout signal depending on the potential variations of the input/output characteristics of the selector can be corrected. The steady pattern noise caused by the variations in amplifier characteristics can be eliminated.

A photoelectric transducer element used in Figs. 2A to 7 will be described as a supplementary explanation of Figs. lC to lE.

Fig. 8A is a schematic sectional view of a photoelectric transducer cell described in Japanese Patent Laid-Open Gazettes No. l2759/l985 to l2765/l985, and Fig. 8B is an equivalent circuit diagram of the cell.

Referring to Figs. 8A and 8B, photoelectric transducer cells are formed on an n+-type silicon substrate 70l, and each photoelectric transducer cell is electrically insulated from adjacent photoelectric transducer cells by an element isolation region 702 made of SiO_2, SiH_3N_4, or polysilicon.

Each photoelectric transducer cell has the following structure.

A p-type region 704 doped with a p-type impurity is formed on an n--type region 703 formed by an epitaxial technique and having a low impurity concentration. An n+-type region 705 is formed in the p-type region 704 by impurity diffusion or ion implantation. The p-type region 704 and the n+-type region 705 respectively serve as the base and emitter of a bipolar transistor.

An oxide film 706 is formed on the n--type region 703, and a capacitor electrode 707 having a predetermined area is formed on the oxide film 706. The capacitor electrode 707 opposes the p-type region 704 through the oxide film 706 and controls a potential of the p-type region 704 floating upon application of a pulse voltage to the capacitor electrode 707.

In addition, an emitter electrode 708 is connected to the n+-type region 705, an n+-type region 7ll having a high impurity concentration is formed on the lower surface of the substrate 70l, and a collector electrode 7l2 is formed to apply a potential to the collector of the bipolar transistor.

The basic operation of the above arrangement will be described. Assume that the p-type region 704 serving as the base of the bipolar transistor is set at a negative potential. Light 7l3 is incident from the side of the p-type region 704. Holes in the electron-hole pairs generated upon radiation are accumulated in the p-type region 7l4 and the potential at the p-type region 7l4 is increased by the accumulated holes in the positive direction (charge accumulation).

Subsequently, a positive read voltage is applied to the capacitor electrode 707, and a read signal corresponding to a change in base potential during charge accumulation is output from the floating emitter electrode 708 (read operation). It should be noted that the amount of accumulated charge is

rarely reduced in the p-type region 704 serving as the base of the bipolar transistor, so that read access can be repeated.

In order to remove the holes from the p-type region 704, the emitter electrode 708 is grounded, and a refresh pulse of a positive voltage is applied to the capacitor electrode 708. Upon application of the refresh pulse, the p-type region 704 is forward-biased with respect to the n+-type region 705, thereby removing the holes. When the refresh pulse falls, the p-type region 704 restores the initial state of the negative potential (refresh operation). Charge accumulation, read access, and refreshing are repeated as described above.

In order to restore the initial potential state of the p-type region 704 by refreshing, a refresh pulse having a sufficient pulse width is required. To the contrary, the refresh pulse width must be shortened to achieve high-speed operation. In this case, when the refresh pulse width is short, satisfactory refreshing cannot be performed. Unnecessary components such as a dark signal and drive noise are added to the after image.

Fig. 9 is a graph showing the relationship between a refresh pulse width $\bar{t}$ applied to the photoelectric transducer cell and the photoelectric transducer cell output.

Referring to Fig. 9, an output at t = 0 is a read signal after charge accumulation and represents a read signal having a level corresponding to the intensity of the incident light.

The output level of such a photoelectric transducer is reduced by refreshing. However, the rate of change in output level and the level of the residual image upon refreshing vary depending on the intensity of the incident light.

When identical refreshing is performed, the levels of the residual signals are not constant. When the intensity of the incident light is high, the level of the residual signal is high. In other words, the after image is typically formed.

The residual signal level of high-intensity incident light is higher than that of low-intensity incident light but is greatly lowered as compared with the initial read signal level. The ratio of the unnecessary components contained in the read signal is substantially low. On the contrary, the residual signal level of the low-intensity incident light is low. A decrease in the residual signal level is small as compared with the initial read signal level. Therefore, the ratio of the unnecessary components included in the read signal is high.

Even in the photoelectric transducer cell having the above characteristics, by subtracting the residual signal obtain upon refreshing from the initial read signal, the above-mentioned specific after image components as well as the unnecessary components such as a dark signal and drive noise can be simultaneously removed.

A second embodiment of the present invention will be described below.

Fig. I0 is a circuit diagram for explaining the basic arrangement of an image pickup element according to the second embodiment of the present invention.

Referring to Fig. I0, an emitter electrode 708 of a photoelectric transducer cell S is connected to a vertical line VL and is grounded through a transistor Qr. The vertical line VL is connected to storage capacitors Ctl and Ct2 through corresponding transistors Qtl and Qt2. The capacitors Ctl and Ct2 are connected to output lines 72l and 722 through transistors Qsl and Qs2, respectively. The output lines 72l and 722 are connected to the input terminals of a differential amplifier 72l, respectively.

A pulse φ from a scanning circuit SH is applied to the gate electrodes of the transistors Qsl and Qs2. Pulses φtl and φt2 are applied to the gate electrodes of the transistors Qtl and Qt2, respectively. A pulse φrh is applied to the gate electrode of the transistor Qr. A read or refresh pulse φr is applied to a capacitor electrode 707 of the photoelectric transducer cell S.

The operation of the above arrangement will be described below.

Fig. Il is a timing chart for explaining the operation of the circuit shown in Fig. I0.

The transistors Qtl, Qt2, and Qr are turned on in response to the pulses φtl, φt2, and φrh, respectively, to clear the capacitors Ctl and Ct2 (time interval Tl).

Subsequently, the pulse φr is supplied to the capacitor electrode 707 while the transistor Qtl is kept on. The read signal from the photoelectric transducer cell S is stored in the capacitor Ctl (time interval T2).

The transistor Qtl is turned off while the pulse φr is kept applied to the capacitor electrode 707. The transistor Qr is turned on in response to the pulse φrh. The photoelectric transducer cell S is refreshed in response to the pulse φrh (time interval T3).

Upon completion of refreshing, the transistor Qt2 is turned on in response to the pulse φt2 while the pulse φr is kept applied to the capacitor electrode 707. The residual signal of the photoelectric transducer cell S is stored in the capacitor Ct2 (time interval T4).

When the read and residual signals are stored in the capacitors Ctl and Ct2, respectively, the transistors Qsl and Qs2 are turned on in response to the pulse φ. The read and residual signals are input to the differential amplifier 723 through the corresponding output lines 72l and 722. A signal Vout proportional to the difference between the read and the residual signals is output from the differential amplifier 723 (time interval T5).

As described above, the signal Vout is a signal free from the after image component and the unnecessary components such as a dark signal and drive noise and accurately corresponds to the intensity of the incident light. In particular, unnecessary component removal on the low-intensity side is effective, and an S/N ratio can be greatly increased.

Fig. I2 is a circuit diagram of an image pickup system of this embodiment. The circuit in Fig. I2 has n circuits of Fig. I0.

Referring to Fig. I2, the emitter electrodes 708 of photoelectric transducer cells Sl to Sn are respectively connected to vertical lines VLl to VLn. The same circuits as in Fig. I0 are connected to the vertical lines. The gate electrodes of the transistors

Qr are commonly connected, and the pulse φrh is applied thereto. The gate electrodes of the transistors Qtl and the gate electrodes of the transistor Qt2 are also commonly connected, and the pulses tl and t2 are supplied to the common gate electrodes, respectively.

The gate electrodes of the transistors Qsl and Qs2 corresponding to the photoelectric transducer cells Sl to Sn are connected to the parallel output terminals of the scanning circuit SH and receive the pulses φl to φn, respectively. The transistors Qsl are commonly connected to the output line 72l and the transistors Qs2 are commonly connected to the output line 722. These output lines are grounded through corresponding transistors l03. A reset pulse φhrs is supplied to the gate electrodes of the transistors l03.

A mode of operation of the arrangement described above will be briefly described with reference to Fig. l3A.

Fig. l3 is a timing chart for explaining the operation of the above arrangement.

As already described above, the capacitors Ctl and Ct2 corresponding to each photoelectric transducer cell are cleared during the time interval Tl. During the time interval T2, the read signal from each photoelectric transducer cell is stored in the corresponding capacitor Ctl. During the time interval T3, each photoelectric transducer cell is refreshed. During the time interval T4, the residual signal of each refreshed photoelectric transducer cell is stored in the corresponding capacitor Ct2.

After the read and residual signals of each photoelectric transducer cell are accumulated in the manner described above, the pulse φl from the scanning circuit SH is supplied to the gate electrodes of the transistors Qsl and Qs2. The read and residual signals stored in the capacitors Ctl and Ct2 of the photoelectric transducer cell Sl are read out and appear on the output lines 72l and 722. A difference between these signals is calculated by the differential amplifier 723, thereby removing the unnecessary components and hence obtaining the output signal Vout.

When a signal is output from the photoelectric transducer cell Sl, the transistor l03 is turned on in response to the pulse φhrs, and the charges left on the output lines 72l and 722 are removed.

In the same manner as described above, the read and residual signals of the photoelectric transducer cells S2 to Sn are output from the capacitors Ctl and Ct2 and appear on the output lines 72l and 722 and are subjected to subtractions by the differential amplifier 723, thereby sequentially outputting signals Vout.

Fig. l3B shows another mode of operation of the above arrangement.

During a time interval Ts, the base electrodes of the cells S are reverse-biased to perform charge accumulation. Upon completion of charge accumulation, unnecessary charges on the vertical transfer line VL and the storage capacitor Ctl are removed before the photoelectric transducer signals are transferred to the storage capacitor Ctl within a time interval Tvc.

Refreshing is performed again during a time interval Tcl, and drive noise is transferred to the storage capacitor Ct2 during a time interval Tt2. Thereafter, the cell S is refreshed during a time interval Tc2, and the next charge accumulation cycle is initiated. The photoelectric transducer signal and drive noise which are stored in the storage capacitors Ctl and Ct2 are output onto horizontal signal lines 72l and 722, respectively.

In the above embodiment, the sensor shown in Figs. 8A and 8B is exemplified. However, the present invention is not limited to any specific scheme of the photosensor.

The present invention can be applied to a color image pickup apparatus of a scheme for processing a plurality of horizontal line signals.

Fig. l4 is a circuit diagram of a third embodiment of the present invention, and Fig. l5 is a detailed circuit diagram of a readout circuit Ri in this embodiment. This embodiment exemplifies a scheme for processing a signal of two horizontal lines. This can apply to any scheme for processing a signal of three or more horizontal lines.

Referring to Fig. l4, photosensors S are arranged in an m × n area. Mosaic R, G, and B filters are arranged on the sensor surface.

Column photosensor outputs are respectively output to the readout circuits Rl to Rn through vertical lines VLl to VLn.

Referring to Fig. l5, in any readout circuit Ri (i = l, 2, ... n), the vertical lines VLi are connected to storage capacitors Ctl to Ct4 through transistors Qtl to Qt4, and the capacitors Ctl to Ct4 are connected to output lines 80l to 804 through transistors Qsl to Qs4, respectively. Since the scheme for processing a signal of two horizontal lines is used, two capacitors for storing the read signals and other two capacitors for storing residual signals are formed.

The gate electrodes of the transistors Qtl to Qt4 are commonly connected through corresponding readout circuits Rl to R4. Pulses φl to φ4 are supplied to the gate circuits of the transistors Qtl to Qt4.

A pulse φi from a horizontal scanning circuit SH is supplied to the transistors Qsl to Qs4 of the readout circuit Ri. The transistors Qsl to Qs4 are simultaneously turned on/off.

The output lines 80l and 802 are connected to the input terminals of a differential amplifier 805, and the output lines 803 and 804 are connected to the input terminals of a differential amplifier 806. Signals OUTl and OUT2 are output from the differential amplifiers 805 and 806, respectively.

Two lines per field are selected by a vertical scanning circuit 807 and an interlace circuit 808. Pairs of two horizontal scanning lines in units of fields are selected in response to pulses Vrl and Vr2.

The operation of the above circuit will be described with reference to Fig. l6.

Fig. l6 is a timing chart for explaining the operation of the above circuit.

Each photosensor read signal and its residual signal for two horizontal lines are read out during a horizontal blanking (HBLK) period and are stored in the storage capacitors in the readout circuits Rl to

Rn. Transfer of one of the two horizontal lines is performed during a time interval Ta in response to the pulse Vrl. Transfer of the remaining horizontal line is performed during a time interval Tb in response to the pulse Vr2.

The transfer operations are substantially the same as those in Fig. l2. However, since transfer is performed during the HBLK period, the transfer time can be shortened as compared with a scheme for processing a signal of one horizontal line. Clearing of the residual signal storage capacitor and its charge accumulation are performed during substantially equal time intervals T3′ and T3″. Smear generated during signal transfer is proportional to the transfer time. In this sense, T2 (T2′) and T3′ (T3″) are shortened to suppress the smearing phenomenon.

The capacitors Ctl and Ct2 are cleared within a time interval Tl in the time interval Ta. During a time interval T2, a pulse φrl is supplied to the first horizontal line in response to the pulse Vrl, and read signals of the photosensors on the first horizontal line are stored in the capacitors Ctl in the readout circuits Rl to Rn. Subsequently, during a time interval T3′, the photosensors of the first horizontal line are refreshed, and the residual signals upon completion of refreshing are stored in the capacitors Ct2.

During the next time interval Tb, the same transfer as in the first horizontal line is performed for the second horizontal line in response to the pulse φr2 generated in response to the pulse Vr2. The read and residual signal of each photosensor for the second horizontal line are respectively stored in the capacitors Ct3 and Ct4.

When the read and residual signals of the first and second horizontal lines are stored in the capacitors Ctl to Ct4 of the readout circuits Rl to Rn, the pulses φl to φn from the horizontal scanning circuit SH are sequentially output to the readout circuits Rl to Rn, so that an R- and G-dot sequential signal OUTl and a G- and B-dot sequential signal OUT2 which are free from the unnecessary components are output from the differential amplifiers 805 and 806, respectively. It should be noted that the signal OUTl is a G- and B-dot sequential signal and the signal OUT2 is an R- and G-dot sequential signal in the next field.

Fig. l7 is a schematic block diagram of an image pickup system using the solid state image pickup apparatus as an image pickup device.

An image pickup device 90l comprises an image pickup apparatus shown in Figs. l4 and l5. The output signals OUTl and OUT2 from the image pickup device 90l are processed by an image processing circuit 903 through a sample/hold (S/H) circuit 902 to produce a standard television signal such as an NTSC signal.

Pulses for driving the image pickup device 90l are supplied from a driver 904. The driver 904 is controlled by a control unit 905. The control unit 905 also controls an exposure control unit 906 to determine an intensity of light incident on the image pickup device 50l.

According to the image pickup apparatus according to the third embodiment of the present, as described above, the residual signal is subtracted from the read signal of the photoelectric transducer cell upon its refreshing to remove the unnecessary components (e.g., a dark signal and drive noise) of the photoelectric transducer element, thereby obtaining a video signal having a high S/N ratio. As a result, a low-cost, compact image pickup apparatus can be manufactured.

Fig. l8 is a schematic view of an area sensor for simultaneously reading out signals of two horizontal lines. This circuit includes switching transistors Trll to Tr22, bipolar transistors B-Trl0 and B-Tr20, and capacitors Coxl0 and Cox20. In this sensor, a photoelectric transducer signal and drive noise of the bipolar transistor B-Trl0 are respectively stored in the capacitors Ctl and Ct2. A photoelectric transducer signal and drive noise of the bipolar transistor B-Tr20 are respectively stored in the capacitors Ct3 and Ct4. When these signals are to be read out, the photoelectric transducer signals are simultaneously and independently read out onto horizontal signal lines S2 and S3, and drive noise components are simultaneously output onto the horizontal signal line Sl. Therefore, the drive noise components are output as a sum signal. R and G filters in an order of R, G, R, G, ... are formed on photoelectric transducer elements of the even-numbered rows, and G and B filters in an order of G, B, G, B, ... are arranged on photoelectric transducer elements of the odd-numbered rows.

Fig. l9 shows an image pickup system using the area sensor shown in Fig. l8.

The image pickup system includes an inversion amplifier 60, an adder 70, a color separation circuit 80, a color image signal processing system 90, an area sensor l0′, a driver 20′, and a clock generator 30′.

Photoelectric transducer signals S2 and S3 read out from the area sensor l0′ are input to the adder 70 and are averaged, thereby obtaining a signal in the form of R + 2G + B. The drive noise is inverted by the inversion amplifier 60, and the inverted signal is input to the adder 70. The adder 70 subtracts the drive noise from the photoelectric transducer signal, thereby producing a luminance signal Y consisting of only an information signal.

The color separation circuit 80 receives the photoelectric transducer signals Sl and S2 and separates them into chrominance signals R, G, and B. The resultant signals Y, R, G, and B are processed by the color image signal processing system 90. The processing system 90 generates a standard television signal such as an NTSC signal.

In the above embodiment, the scheme for simultaneously reading out signals of two horizontal lines is used. However, the present invention is applicable to a scheme for simultaneously reading out signals of three horizontal signals.

The storage capacitors can be omitted if the image pickup apparatus includes a shutter.

A subtracter for removing the drive noise may be connected to the output terminal within the apparatus.

In the above embodiment, the drive noise can be output independently of the photoelectric transducer signal, so that an external large-capacity memory need not be arranged.

In the horizontal line readout scheme, since the noise components can be added and its sum can be output, the number of horizontal signal lines can be reduced. Therefore, a multi horizontal line readout scheme can be easily achieved.

Fig. 20 shows still another embodiment of the present invention. In this embodiment, the differential amplifier 723 in Fig. I0 is replaced with a clamp circuit. The same reference numerals as in Figs. I to I9 denote the same parts in Fig. 20.

Fig. 2I is a timing chart for explaining the operation of the circuit shown in Fig. 20.

Cells S are reverse-biased to perform charge accumulation during a time interval Ts. Upon completion of charge accumulation, the unnecessary charges on the vertical transfer lines VL and in the storage capacitors CtI are removed prior to transfer of photoelectric transducer signals within a time interval Tvc. The photoelectric transducer signal is transferred to a corresponding storage capacitor CtI during the time interval TtI.

Refreshing is performed during a time interval TcI, and drive noise is transferred to the storage capacitor Ct2 during a time interval Tt2. Thereafter, the cells S are refreshed during a time interval of Tc2, and the next charge accumulation cycle is initiated. The photoelectric transducer signals and the drive noise are independently obtained. The signals stored in the storage capacitors CtI and Ct2 are dot-sequentially transferred on a single signal line S in response to drive pulses φsI and φs2. This operation occurs during time intervals TRI and TR2. A drive pulse φhrs is used to reset the signal line to the reference potential. The signal obtained by the above-mentioned read operation represents a waveform of an output Vout. The drive noise and the photoelectric transducer signal are represented by W and S′, respectively.

The dot sequential signal S is input to a clamp circuit I, and only the drive noise N is clamped in accordance with a drive pulse φs2. As a result, the drive noise N is eliminated, and a true information signal indicated by a hatched portion in Fig. 2I can be obtained.

Fig. 22 is a schematic circuit diagram of an area sensor constituted by the photoelectric transducer elements shown in Fig. 20. Referring to Fig. 22, the area sensor includes a vertical shift register V•SR, a horizontal shift register H•SR, and Smn, base accumulation type transistors arranged in an $m \times n$ matrix. The operation of the area sensor is basically the same as that of the photoelectric transducer element shown in Fig. 20, except that the area sensor performs horizontal scanning and vertical scanning, and a detailed description thereof will be omitted. Clamping of the read signal, which is the characteristic feature of this embodiment shown in Fig. 22, will be described in detail.

A schematic waveform of the read signal is shown in Fig. 23. A signal S′ appears on a read signal line S, and a pulse φs2 is a drive pulse. Referring to Fig. 23, drive noise and the photoelectric signal of a cell SII correspond to NI and SI, respectively. A cell SI2 outputs signals N2 and S2, a cell SI3 outputs signals N3 and S3, a cell SI4 outputs signals N4 and S4, ... The drive noise component of the dot sequential signal is clamped in response to the drive pulse φs2. As a result, the drive noise is removed, and only the true information signal can be obtained.

The above embodiment exemplifies a scheme for reading out a signal of one horizontal line. However, this embodiment may be applied to a scheme for reading out a signal of one horizontal line in a time-divisional manner or a scheme for simultaneously reading signals of a plurality of horizontal lines, as shown in Fig. I4.

The base accumulation type transistor is exemplified as the photoelectric transducer element. However, a MOS or SIT image pickup device may be used as the photoelectric transducer element.

In the above embodiment, the drive noise and the photoelectric tansducer signal are converted into a dot sequential signal, and clamping can be easily performed, thereby easily removing the drive noise.

Claims

I. An image pickup apparatus including:

a) a plurality of photoelectric transducer elements for converting incident light into electrical signals;

b) a plurality of amplifying means for respectively amplifying electrical signals from said plurality of photoelectric transducer elements; and

c) operating means having a first mode for causing said amplifying means to amplify the electrical signals from said photoelectric transducer elements and for forming a first signal, and a second mode for causing said amplifying means to amplify a reference signal and forming a second signal.

2. An apparatus according to claim I, wherein said photoelectric transducer element includes a transistor.

3. An apparatus according to claim I, wherein said operating means includes a differential amplifier.

4. An apparatus according to claim I, wherein said operating means includes a clamp circuit.

5. An apparatus according to claim I, wherein said operating means comprises holding means for holding at least one of the first and second signals.

6. An apparatus according to claim 5, wherein said holding means includes a capacitor.

7. An apparatus according to claim 5, wherein said holding means includes a sample/hold circuit.

8. An apparatus according to claim I, wherein the reference signal is a part of the electrical signal output from said photoelectric transducer element.

9. An image pickup apparatus including:

a) a plurality of photoelectric transducer elements for converting incident light into electrical signals; and

b) operating means having a first mode for reading out as a first signal an electrical signal corresponding to light incident on said photoelectric transducer elements and a second mode for reading out as a second signal an electrical signal which does not correspond to the light incident on said photoelectric transducer elements, said operating means being adapted to perform an arithmetic operation of the first and second signals read out in the first and second modes.

10. An apparatus according to claim 9, wherein said photoelectric transducer element includes a transistor.

11. An apparatus according to claim 9, wherein said operating means includes a differential amplifier.

12. An apparatus according to claim 9, wherein said operating means includes a clamp circuit.

13. An apparatus according to claim 9, wherein said operating means comprises holding means for holding at least one of the first and second signals.

14. An apparatus according to claim 13, wherein said holding means includes a capacitor.

15. An apparatus according to claim 13, wherein said holding means includes a sample/hold circuit.

16. An apparatus according to claim 9, wherein read access in the second mode is performed as soon as read access in the first mode is performed.

17. An image pickup apparatus including:

a) a plurality of photoelectric transducer elements for converting incident light into electrical signals;

b) photoelectric transducer element control means having a first mode for reading out as a first signal an electrical signal corresponding to light incident on said photoelectric transducer elements and a second mode for reading out as a second signal an electrical signal which does not correspond to the light incident on said photoelectric transducer elements;

c) storage means for independently storing the first and second signals; and

d) operating means for operating the first and second signals stored in said storage means.

18. An apparatus according to claim 17, wherein said storage means includes a capacitor.

19. An apparatus according to claim 17, wherein said photoelectric transducer element includes a transistor.

20. An apparatus according to claim 17, wherein said operating means includes a differential amplifier.

21. An apparatus according to claim 17, wherein said operating means includes a clamp circuit.

22. An apparatus according to claim 17, wherein read access in the second mode is performed as soon as read access in the first mode is performed.

23. An apparatus according to claim 17, wherein said plurality of photoelectric transducer elements are arranged in a matrix form, and said photoelectric transducer element control means scans said plurality of photoelectric transducer elements in row and column directions.

24. An apparatus according to claim 23, wherein said photoelectric element control means simulteneously reads out the electrical signals of photoelectric transducer elements of a plurality of rows in each scanning cycle in the row direction.

25. An apparatus according to claim 24, wherein said photoelectric transducer element control means has a blanking period between the scanning cycles in the row direction.

26. An apparatus according to claim 25, wherein said storage means store the first and second signals of each photoelectric element of the plurality of rows within the blanking period.

27. An apparatus according to claim 26, further comprising signal lines for respectively reading out the signals stored in said storage means.

28. An apparatus according to claim 27, wherein of said signal lines, signal lines for the second signal are commonly connected.

29. Apparatus comprising an information signal source a reference signal source, signal processing means arranged to process the reference signal and the information signal in the same way, and means for combining the processed reference and information signals to produce an information signal in which noise introduced by the signal processing means is reduced.

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FIG.1A

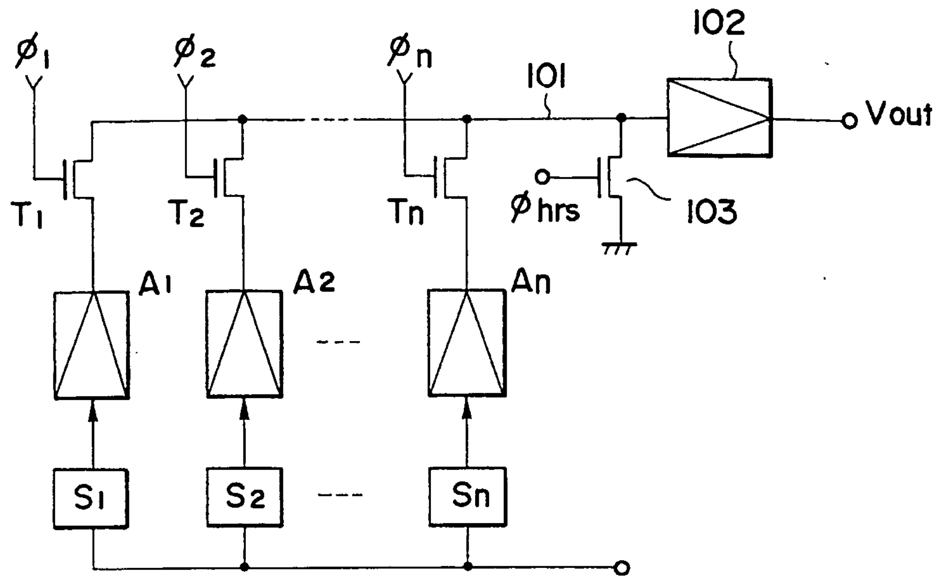


FIG.1B

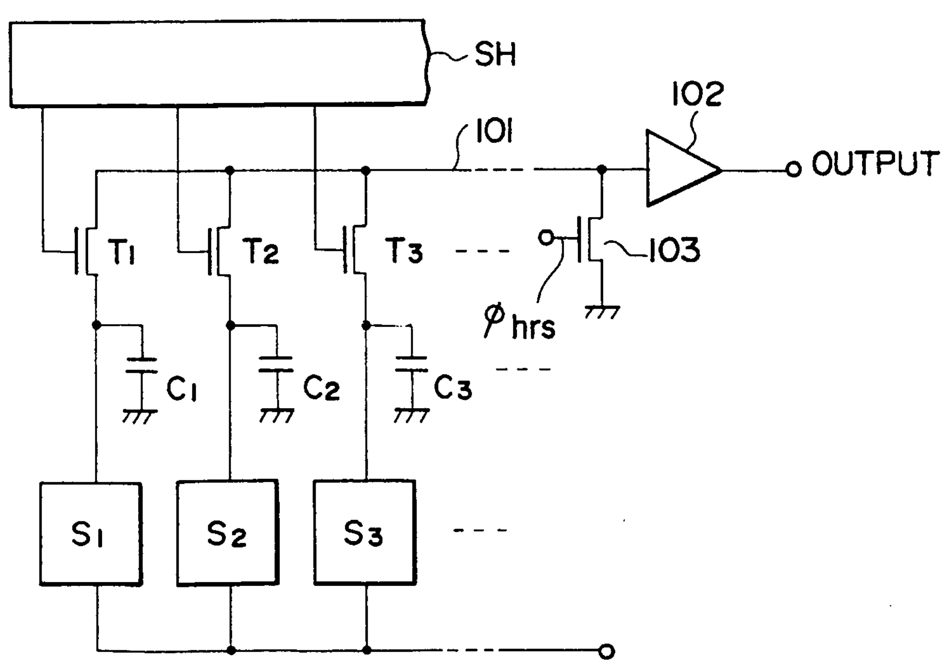


FIG.1C

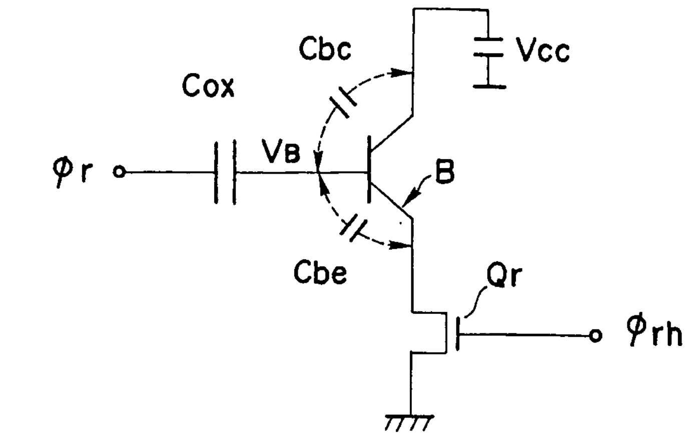


FIG.1D

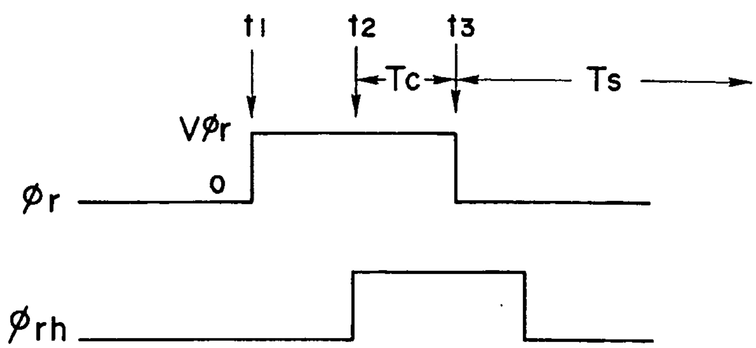


FIG.1E

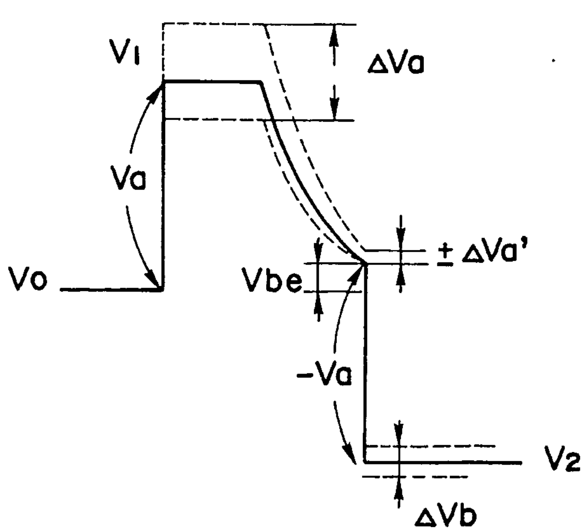


FIG.2A

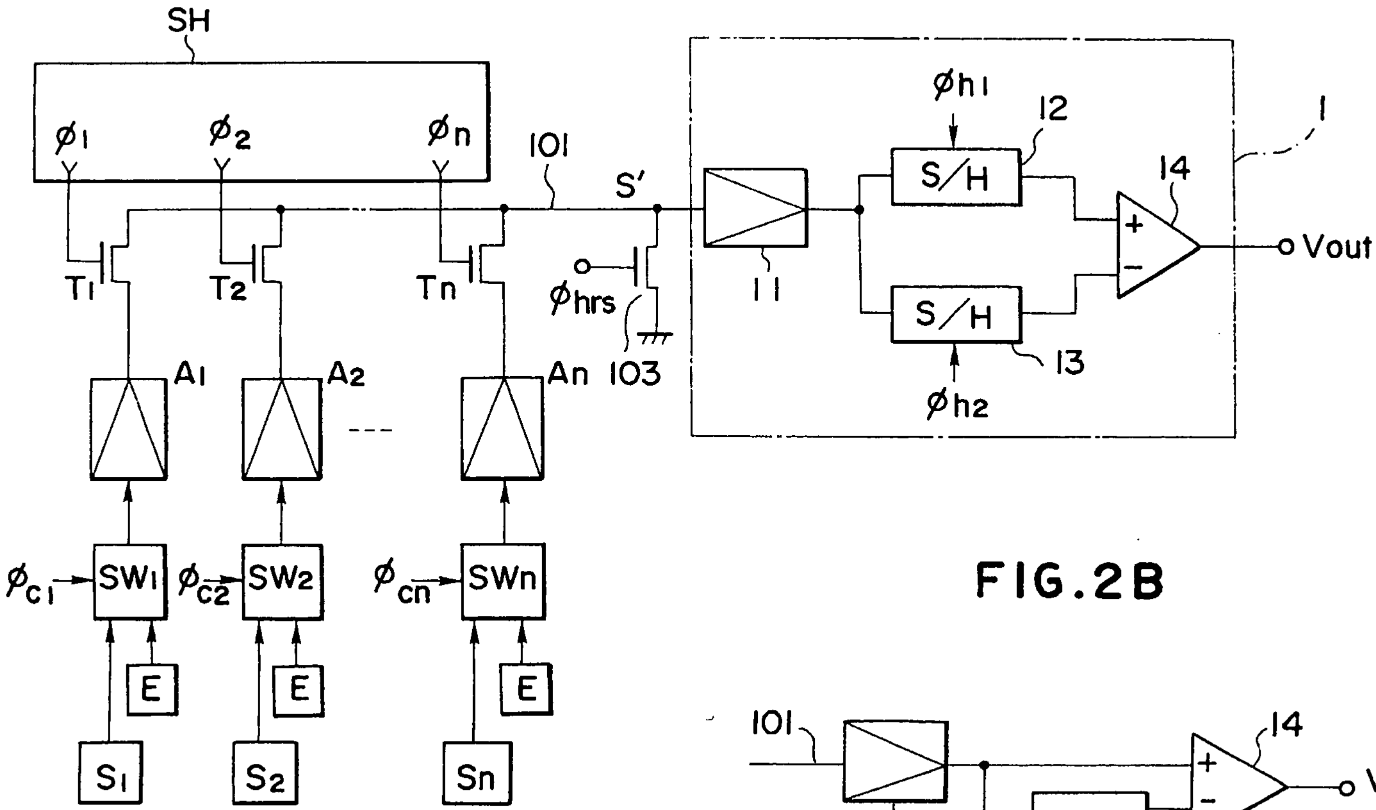

SH
ϕ_1
ϕ_2
ϕ_n
101
S'
T1
T2
Tn
ϕ_{hrs}
103
A1
A2
An
11
ϕ_{h1}
12
S/H
S/H
13
ϕ_{h2}
14
+
−
Vout
1
SW1
SW2
SWn
ϕ_{c1}
ϕ_{c2}
ϕ_{cn}
E
E
E
S1
S2
Sn

FIG.2B

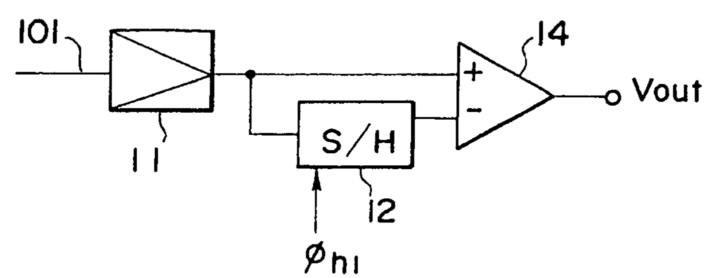

101
11
S/H
12
ϕ_{h1}
14
+
−
Vout

FIG.3

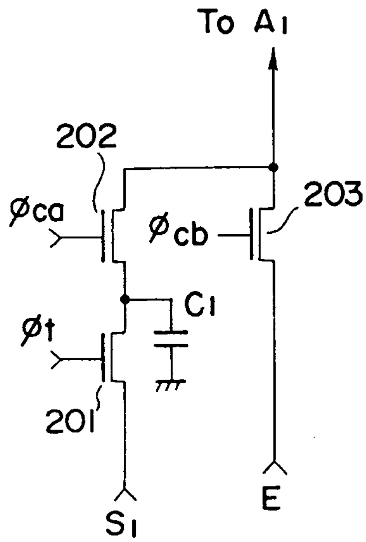


FIG.4

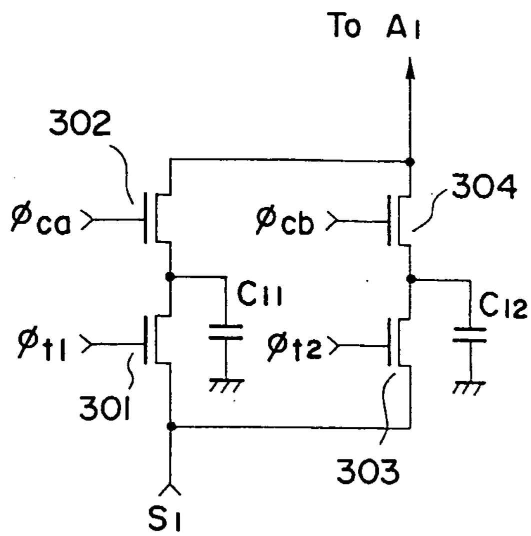


FIG.5A

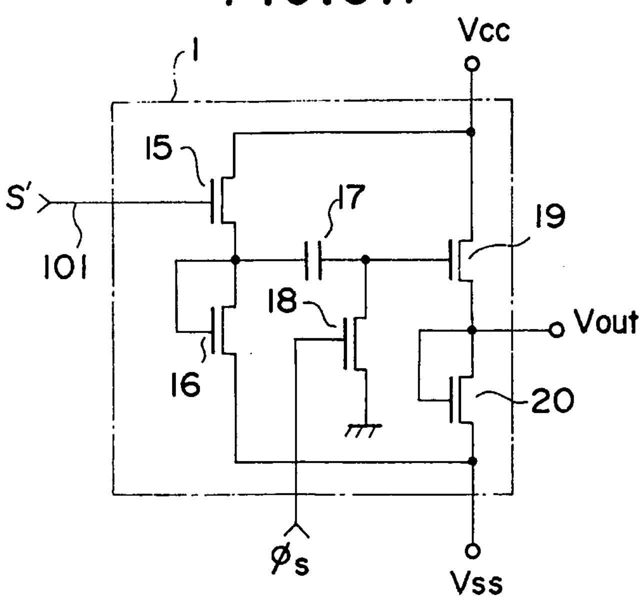


FIG.5B

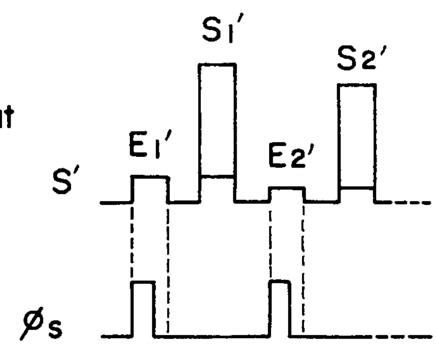


FIG.6A

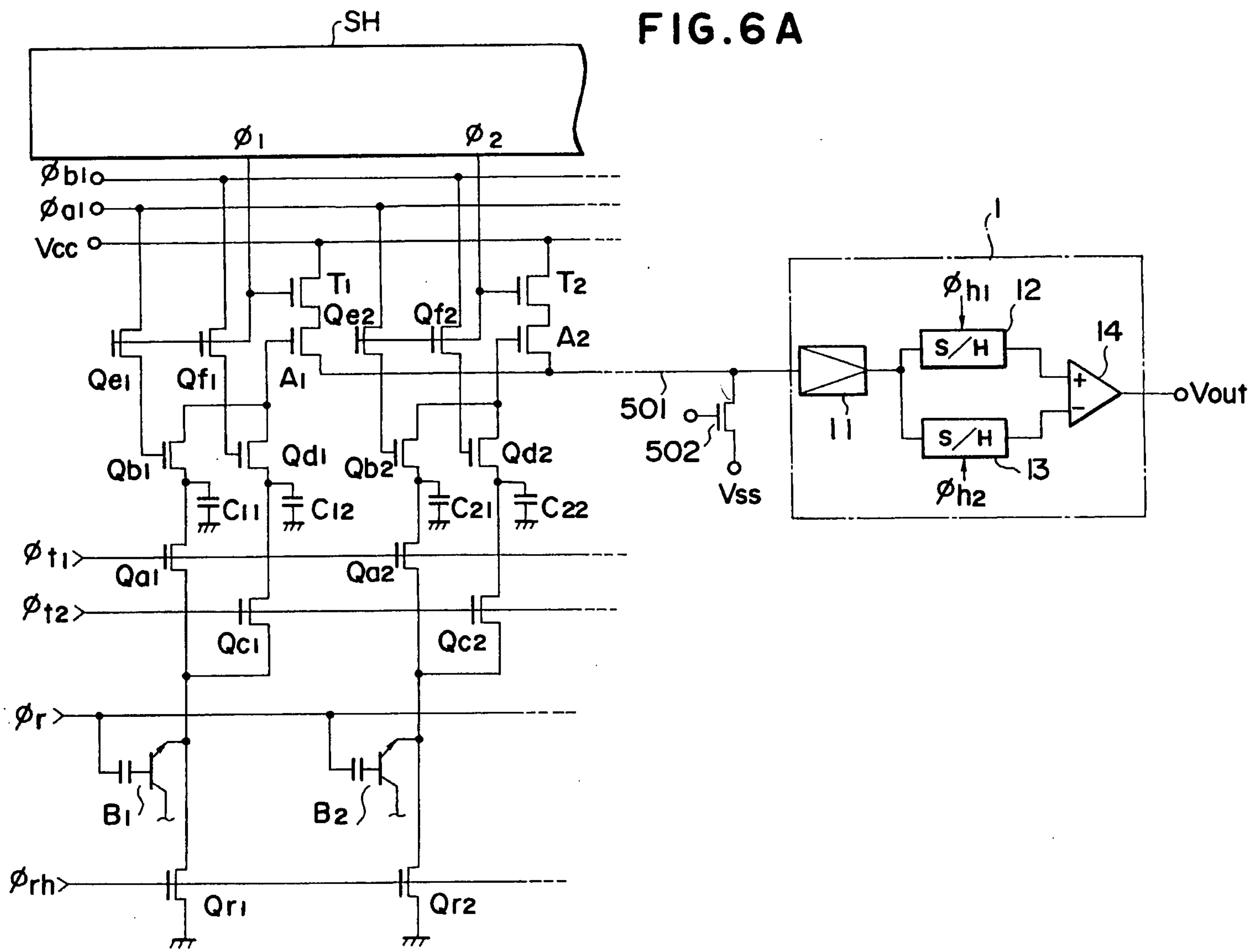

SH
ϕ1
ϕ2
ϕb1
ϕa1
Vcc
T1
T2
Qe1
Qf1
A1
Qe2
Qf2
A2
Qb1
Qd1
Qb2
Qd2
C11
C12
C21
C22
ϕt1
ϕt2
Qa1
Qa2
Qc1
Qc2
ϕr
B1
B2
ϕrh
Qr1
Qr2
501
502
Vss
1
11
ϕh1
ϕh2
S/H
S/H
12
13
14
+
-
Vout

FIG.6B

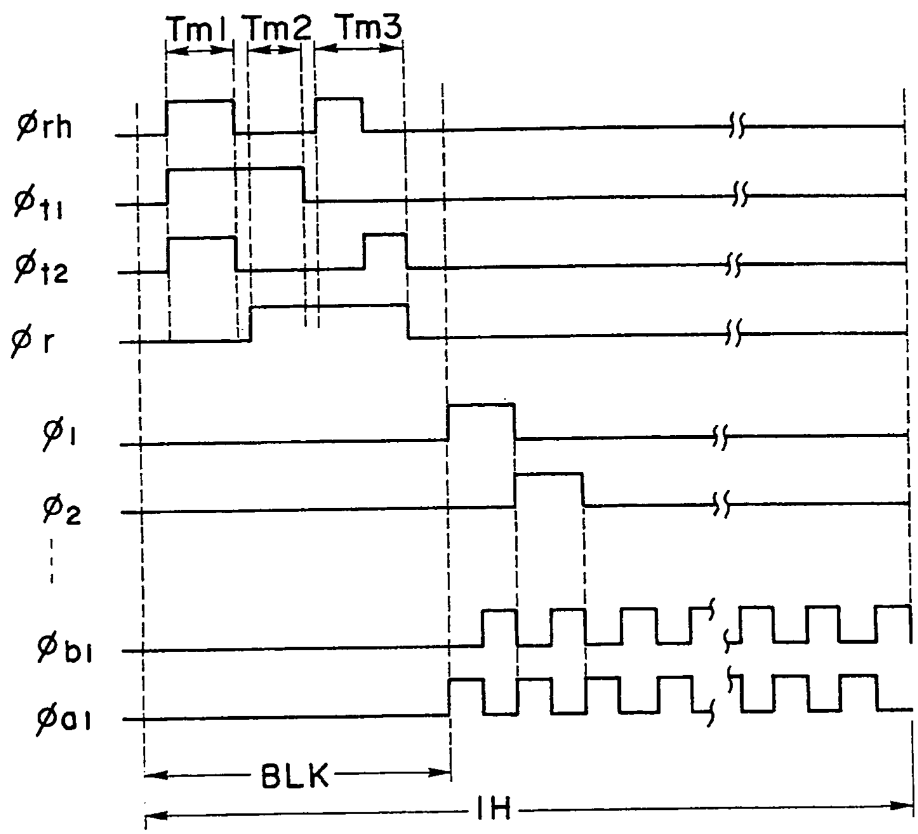


FIG.7

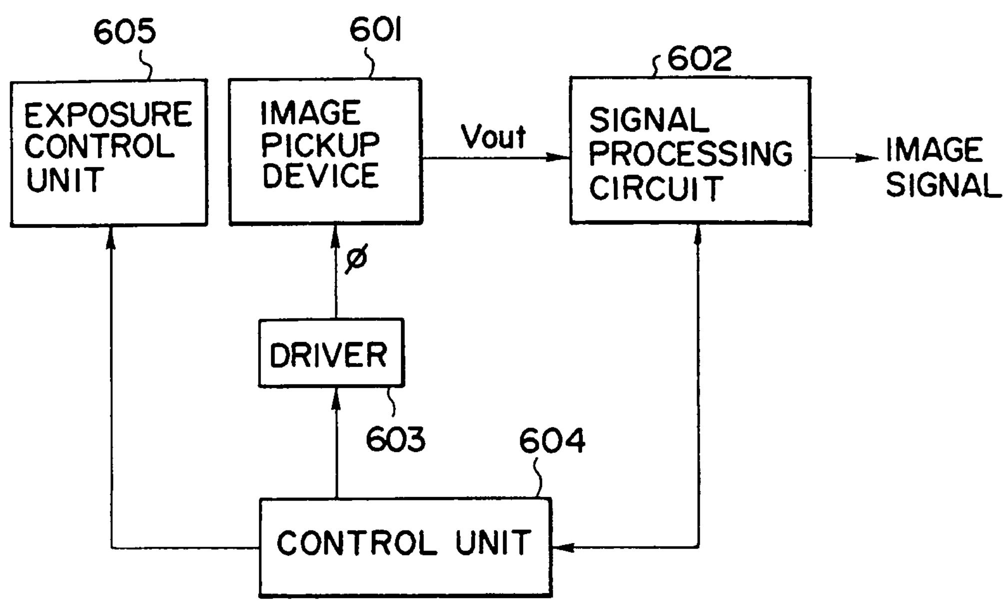
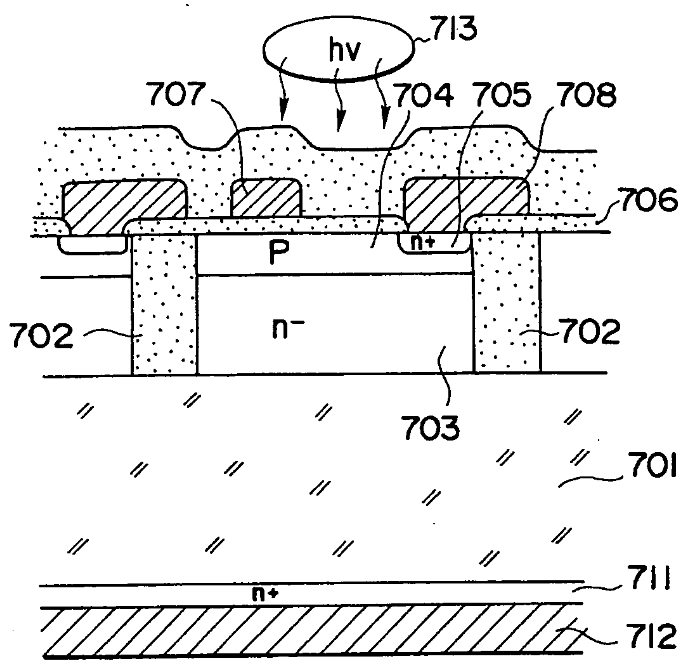
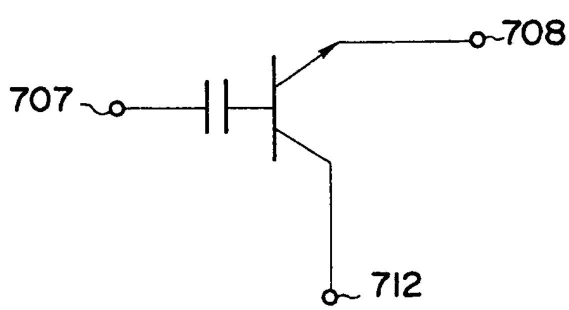

605
601
602
EXPOSURE CONTROL UNIT
IMAGE PICKUP DEVICE
Vout
SIGNAL PROCESSING CIRCUIT
IMAGE SIGNAL
ϕ
DRIVER
603
604
CONTROL UNIT

FIG.8A



hv
713
707
704
705
708
706
P
n+
702
n⁻
702
703
701
711
n+
712

FIG.8B



708
707
712

FIG.9

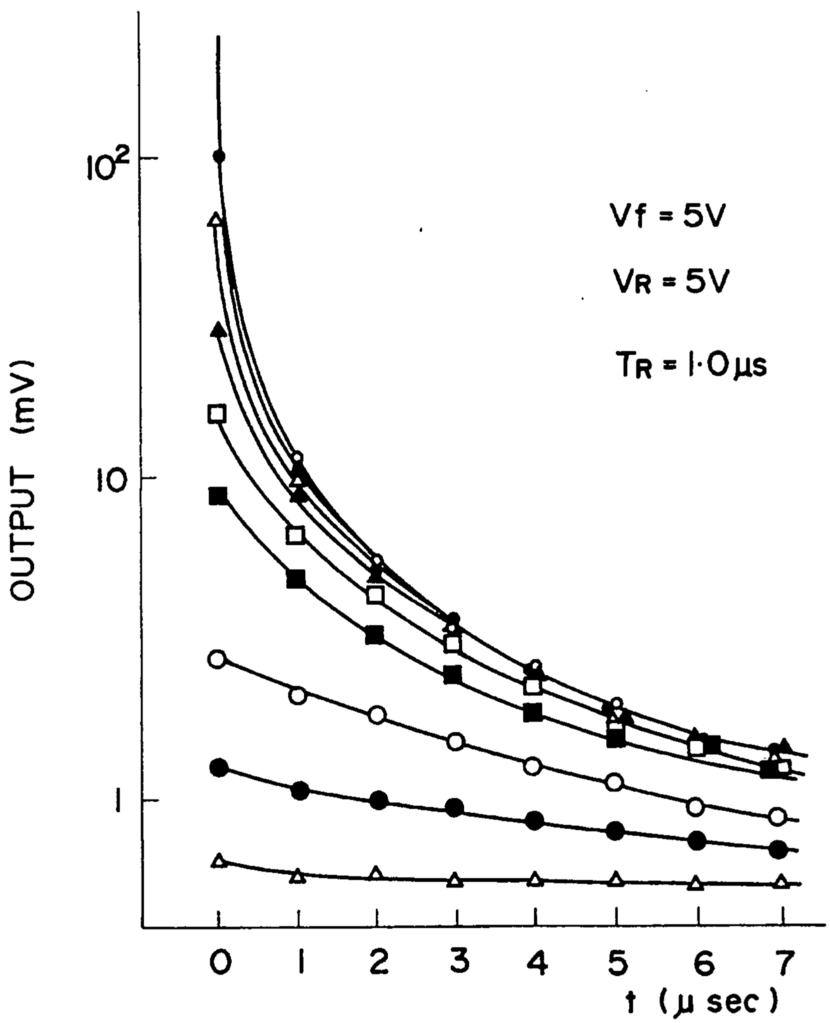
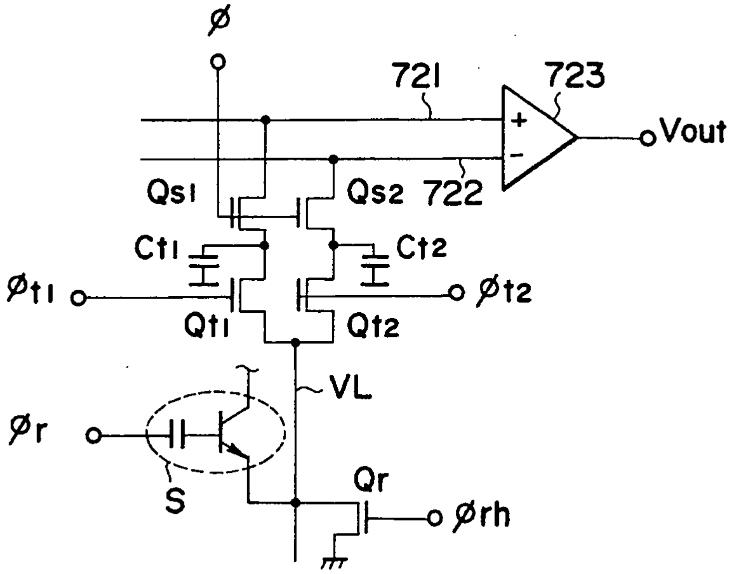
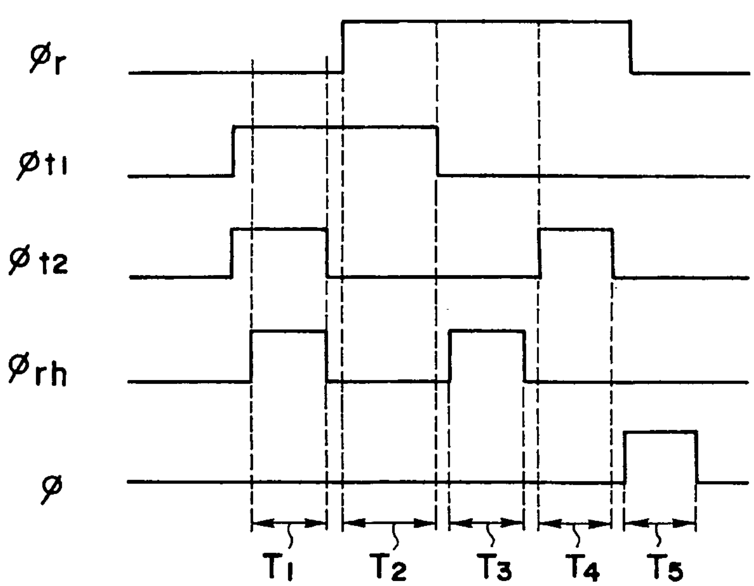


FIG.10



Ø
721
723
Vout
Qs1
Qs2
722
Ct1
Ct2
Øt1
Øt2
Qt1
Qt2
VL
Ør
S
Qr
Ørh

FIG.11



Ør
Øt1
Øt2
Ørh
Ø
T1
T2
T3
T4
T5

FIG.12

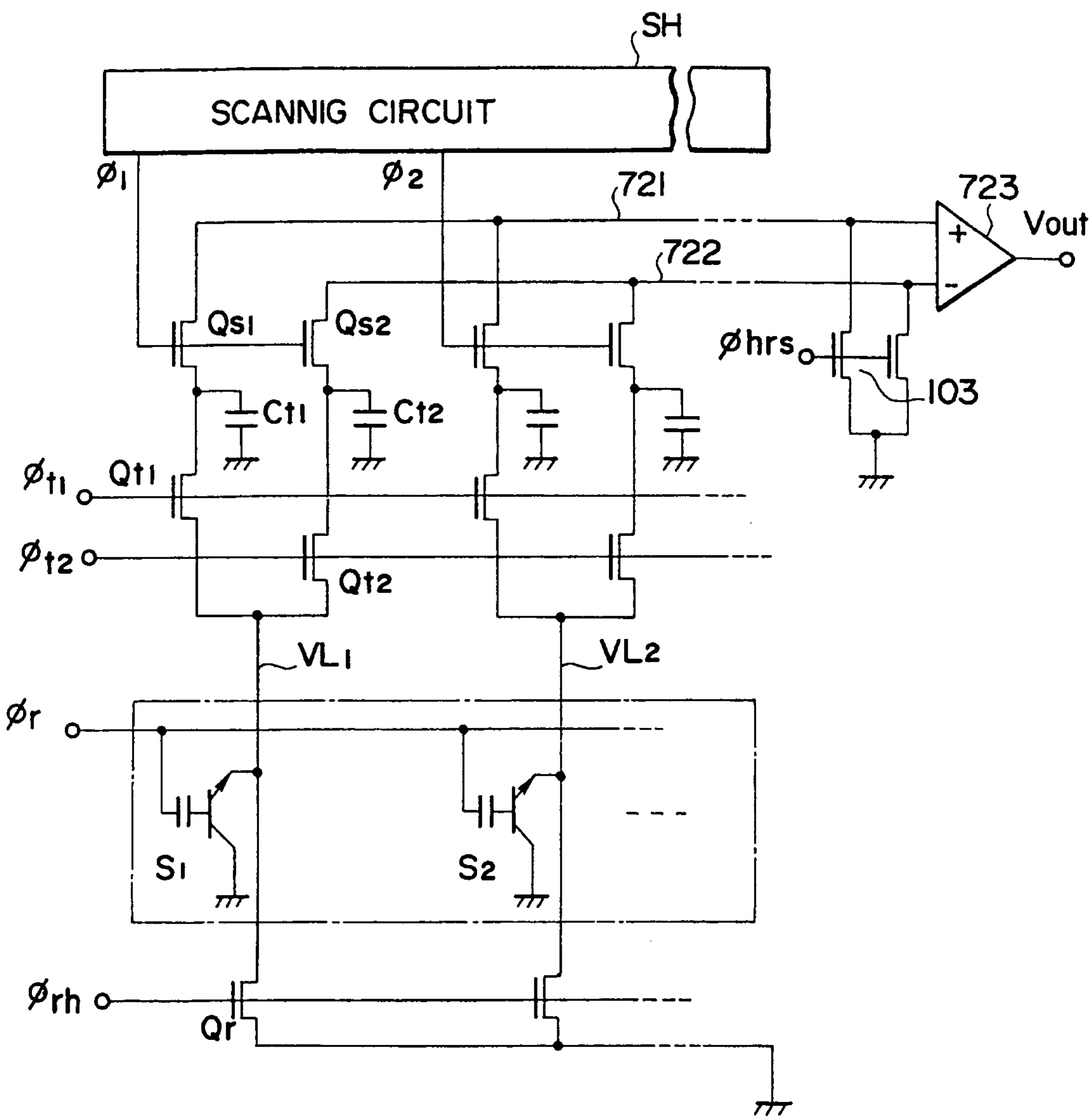

SH
SCANNIG CIRCUIT
Ø1
Ø2
721
722
723
Vout
+
-
Qs1
Qs2
Øhrs
103
Ct1
Ct2
Øt1
Qt1
Øt2
Qt2
VL1
VL2
Ør
S1
S2
Ørh
Qr

FIG.13A

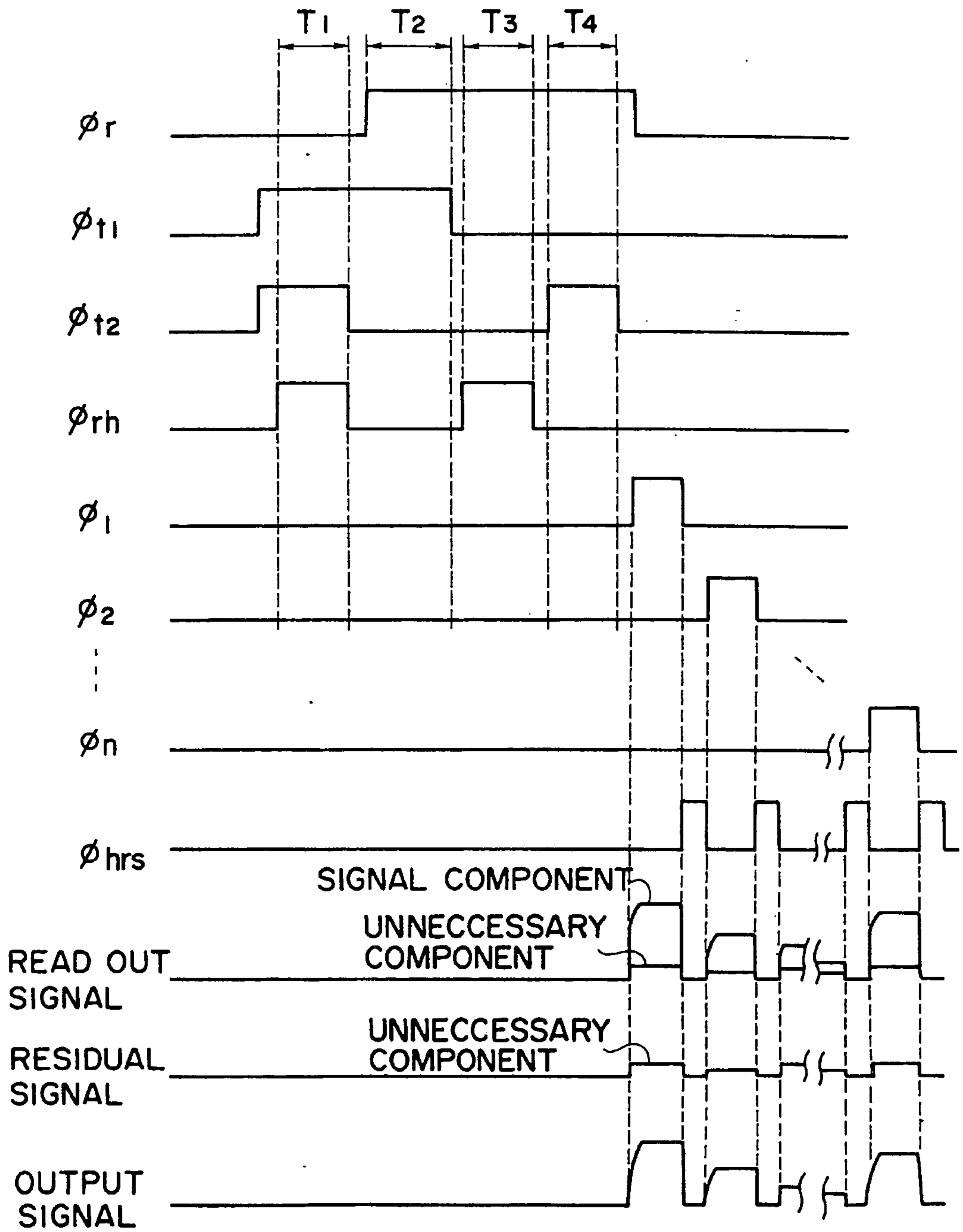

T1
T2
T3
T4
ør
øt1
øt2
ørh
ø1
ø2
øn
øhrs
SIGNAL COMPONENT
UNNECCESSARY COMPONENT
READ OUT SIGNAL
UNNECCESSARY COMPONENT
RESIDUAL SIGNAL
OUTPUT SIGNAL

FIG.13B

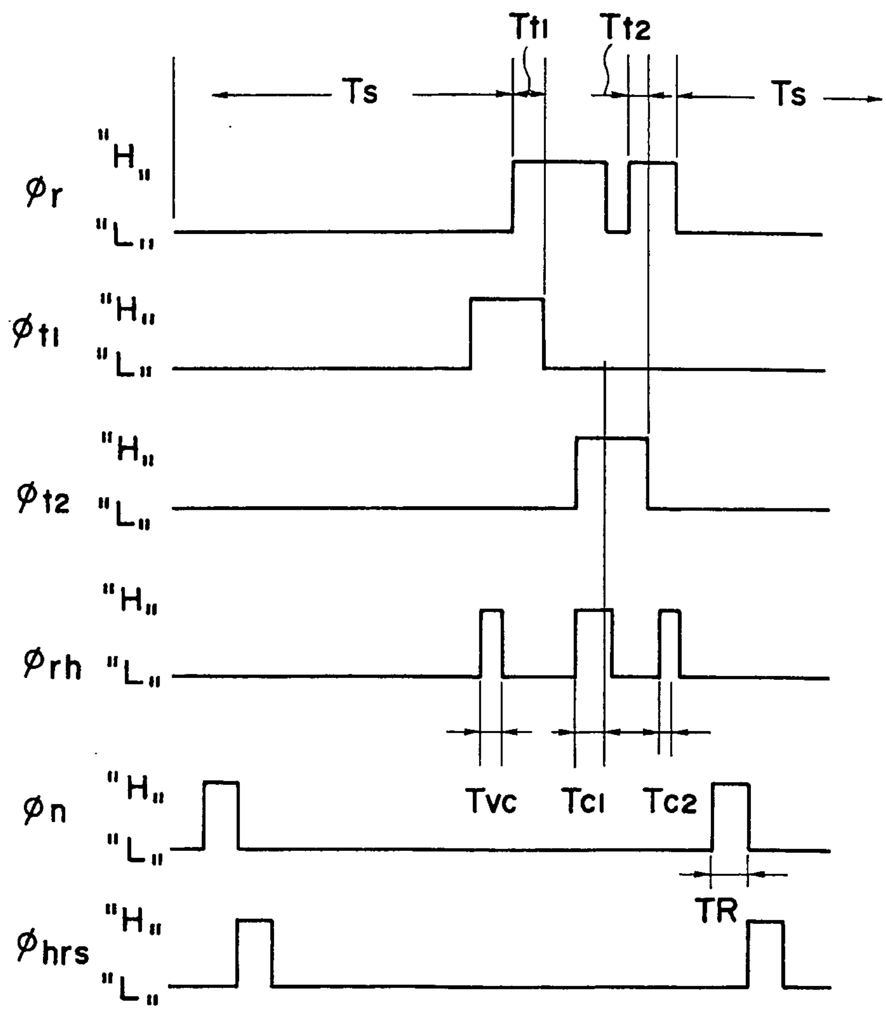
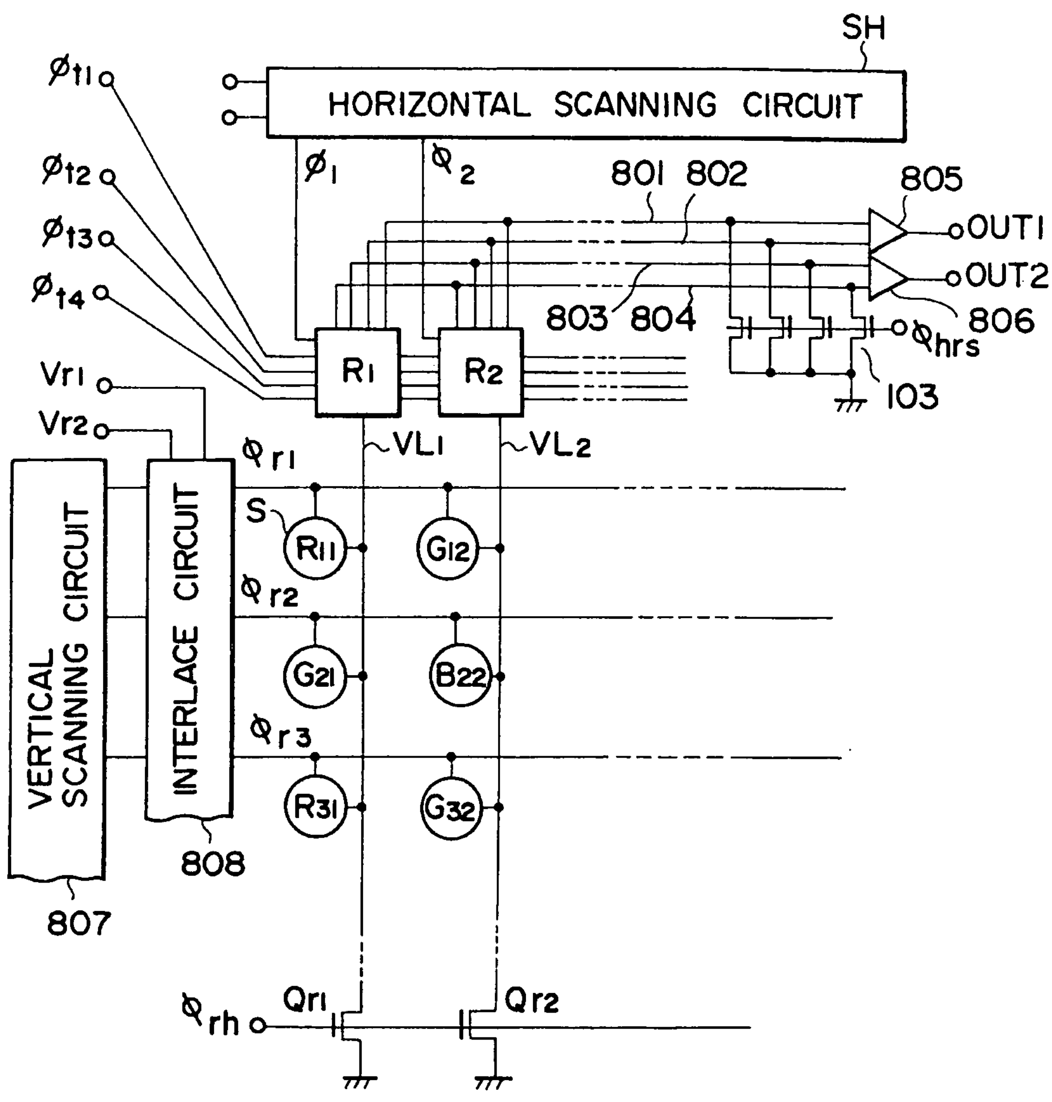
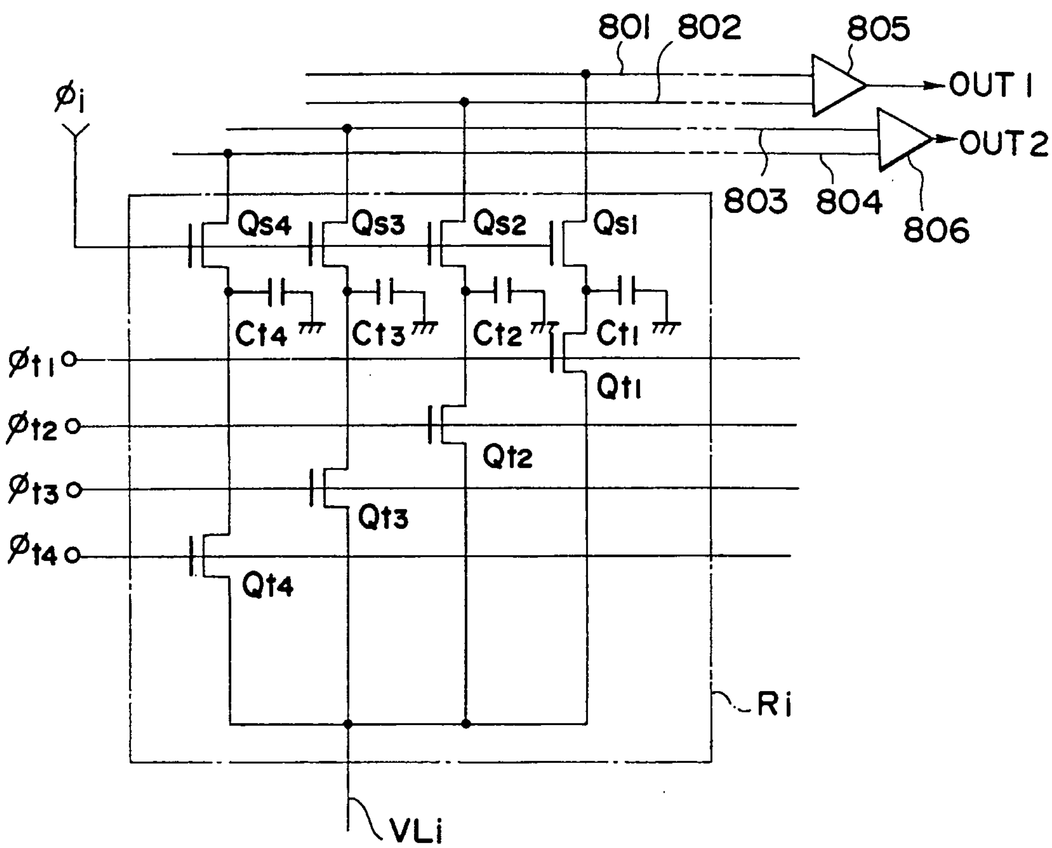

Tt1
Tt2
Ts
Ts
φr
"H"
"L"
φt1
"H"
"L"
φt2
"H"
"L"
φrh
"H"
"L"
Tvc
Tc1
Tc2
φn
"H"
"L"
TR
φhrs
"H"
"L"

FIG.14



SH
HORIZONTAL SCANNING CIRCUIT
φt1
φt2
φt3
φt4
φ1
φ2
801 802
805
OUT1
OUT2
803 804
806
φhrs
103
R1
R2
Vr1
Vr2
φr1
VL1
VL2
S
R11
G12
φr2
G21
B22
φr3
R31
G32
VERTICAL SCANNING CIRCUIT
INTERLACE CIRCUIT
808
807
φrh
Qr1
Qr2

FIG.15



801
802
805
OUT 1
OUT 2
803
804
806
ϕ_i
Qs4
Qs3
Qs2
Qs1
Ct4
Ct3
Ct2
Ct1
ϕ_{t1}
ϕ_{t2}
ϕ_{t3}
ϕ_{t4}
Qt1
Qt2
Qt3
Qt4
Ri
VLi

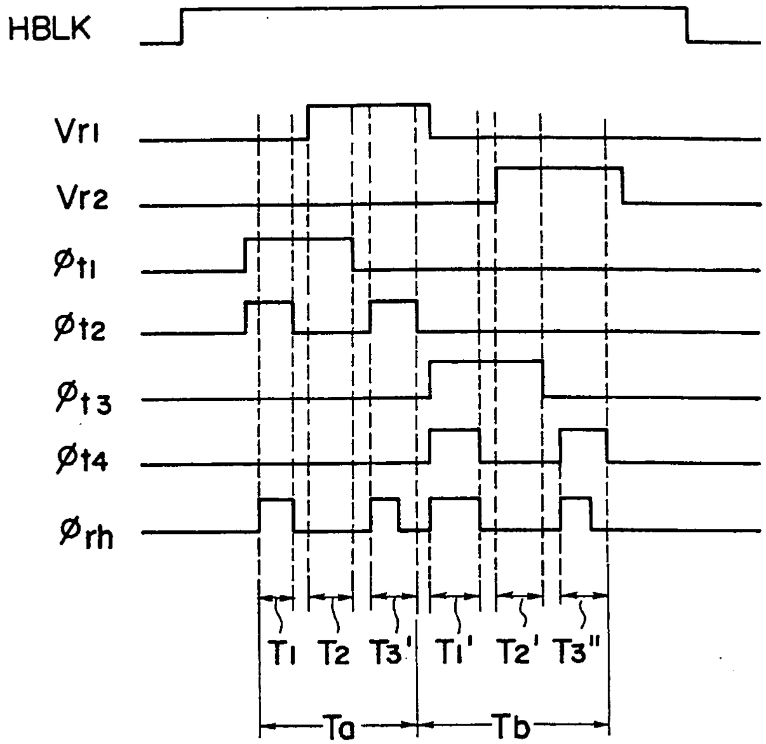

HBLK
Vr1
Vr2
ϕ_{t1}
ϕ_{t2}
ϕ_{t3}
ϕ_{t4}
ϕ_{rh}
T1 T2 T3' T1' T2' T3''
Ta
Tb

FIG.16

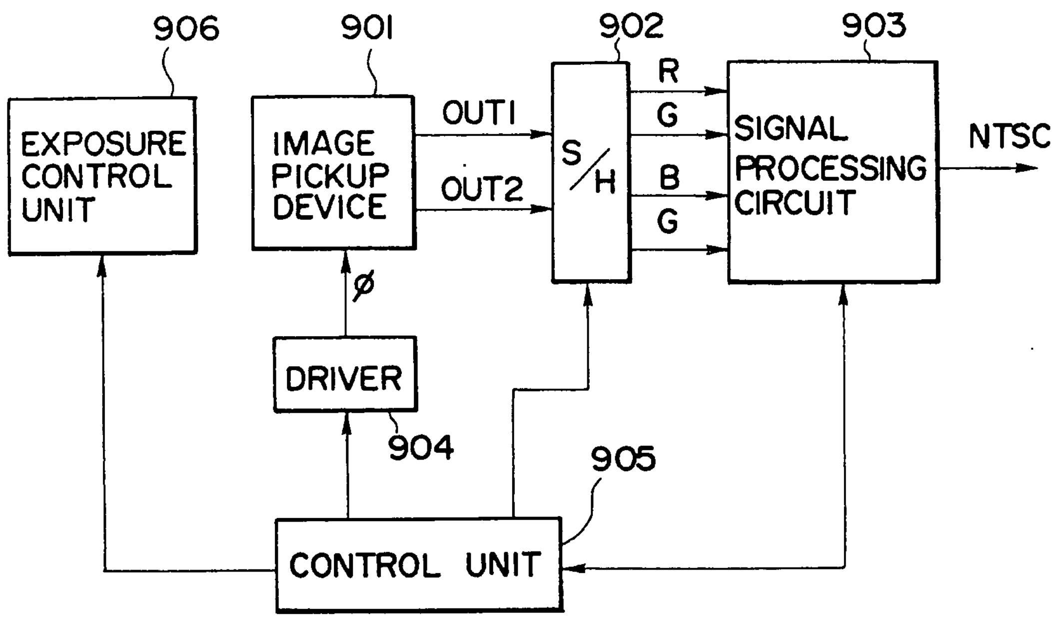

906
EXPOSURE CONTROL UNIT
901
IMAGE PICKUP DEVICE
OUT1
OUT2
902
S/H
R
G
B
G
903
SIGNAL PROCESSING CIRCUIT
NTSC
ϕ
DRIVER
904
905
CONTROL UNIT

FIG.17

FIG.18

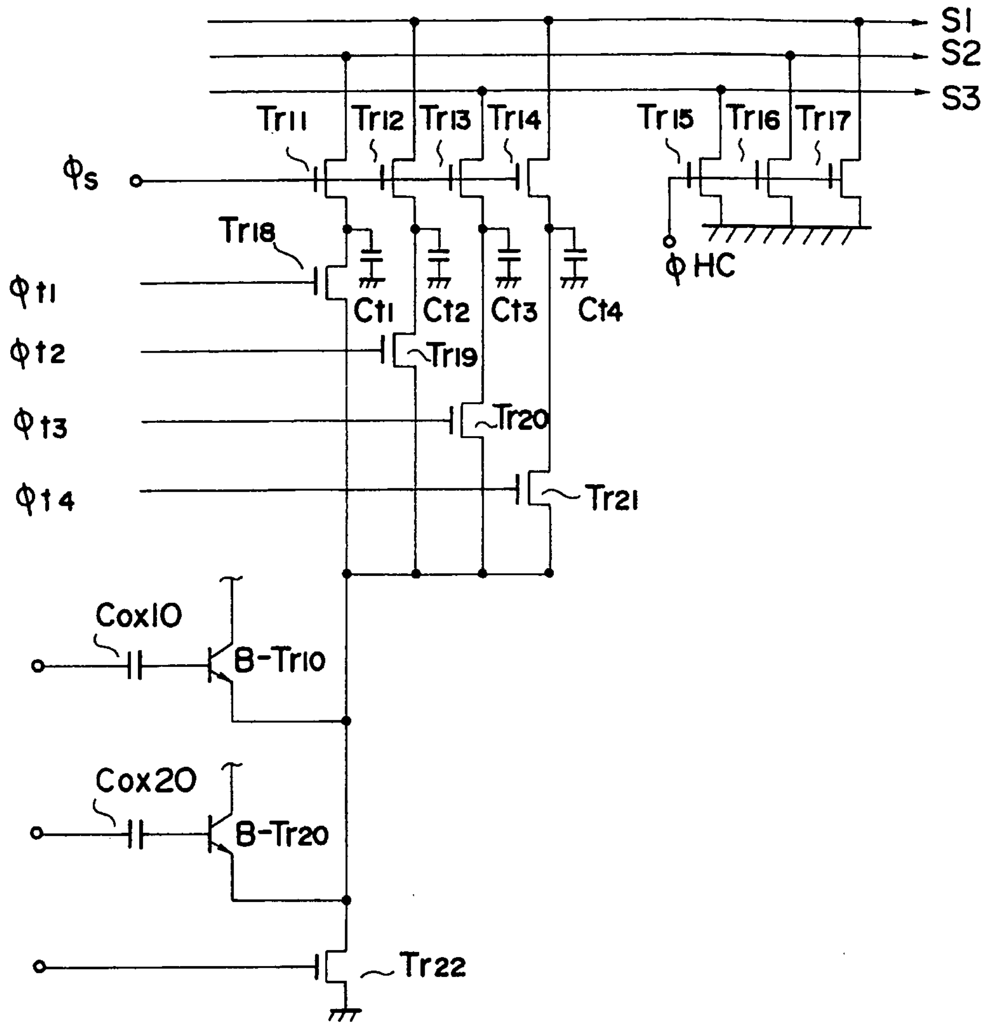
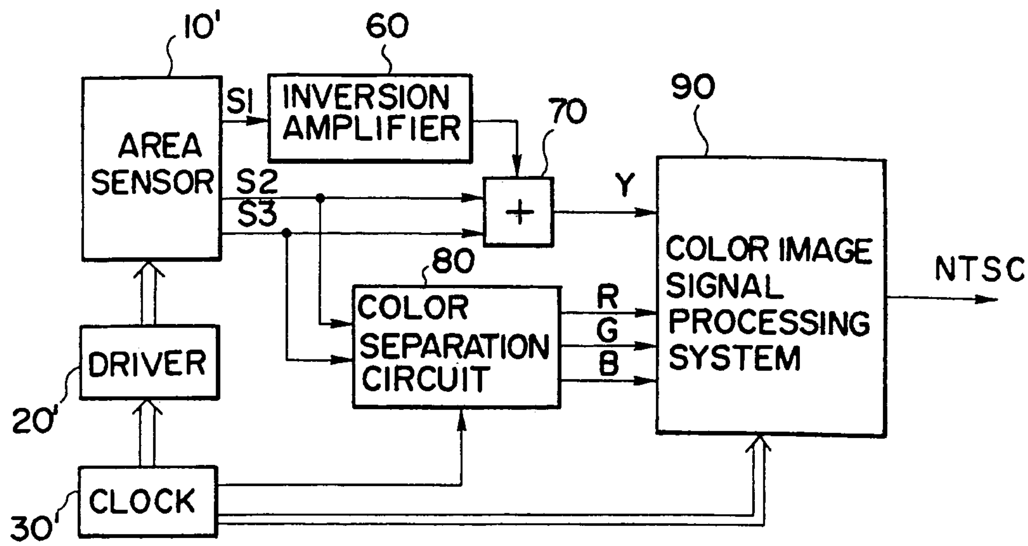
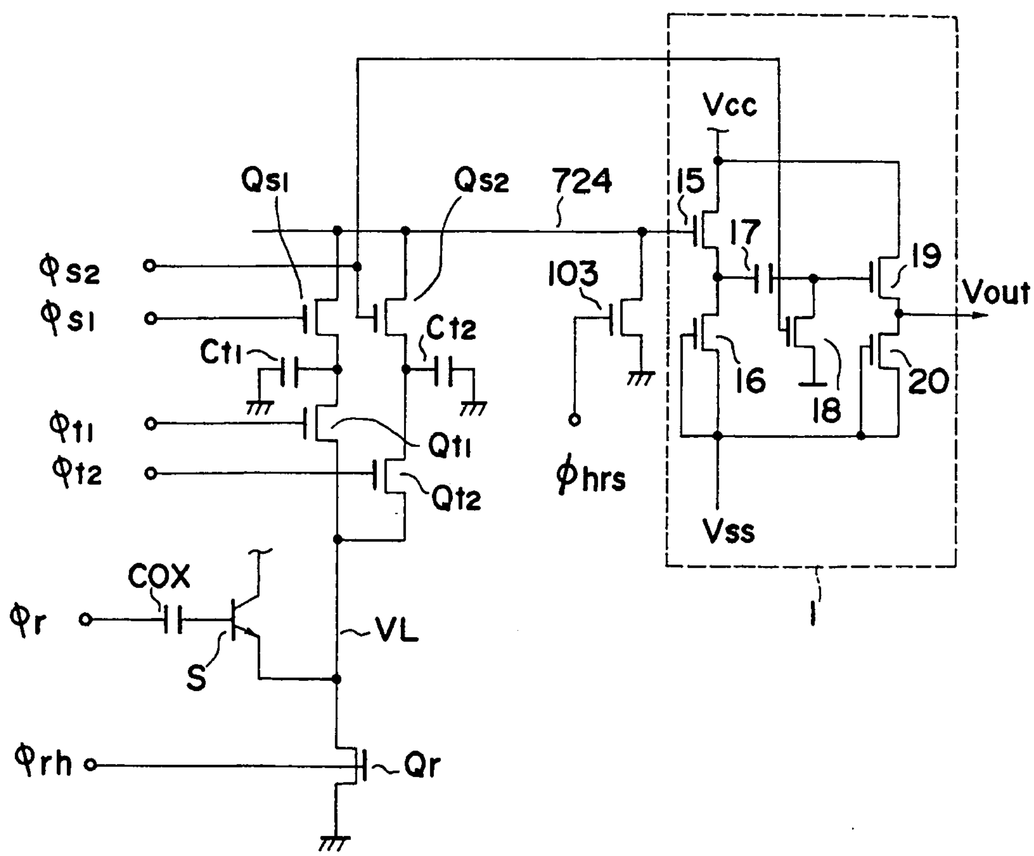

S1
S2
S3
Tr11
Tr12
Tr13
Tr14
Tr15
Tr16
Tr17
φs
Tr18
φHC
φt1
Ct1
Ct2
Ct3
Ct4
φt2
Tr19
φt3
Tr20
φt4
Tr21
Cox10
B-Tr10
Cox20
B-Tr20
Tr22

FIG.19



10'
60
S1
INVERSION AMPLIFIER
70
90
AREA SENSOR
S2
S3
+
Y
COLOR IMAGE SIGNAL PROCESSING SYSTEM
NTSC
80
COLOR SEPARATION CIRCUIT
R
G
B
DRIVER
20'
CLOCK
30'

FIG.20



Vcc
Qs1
Qs2
724
15
17
19
φs2
φs1
103
Vout
Ct1
Ct2
16
20
18
φt1
φt2
Qt1
Qt2
φhrs
Vss
COX
1
φr
VL
S
φrh
Qr

FIG.21

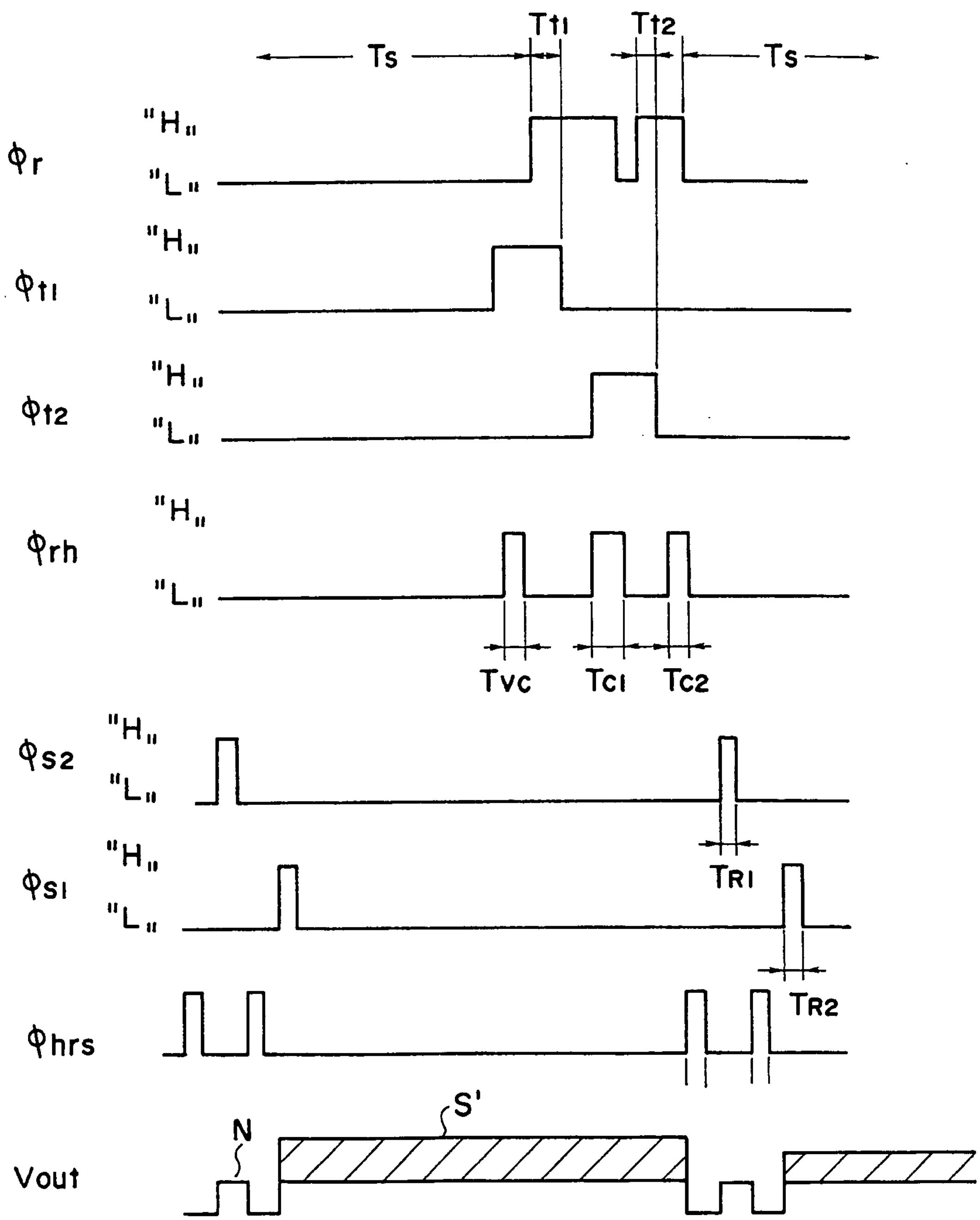

Ts
Tt1
Tt2
Ts
φr
"H"
"L"
φt1
"H"
"L"
φt2
"H"
"L"
φrh
"H"
"L"
Tvc
Tc1
Tc2
φs2
"H"
"L"
TR1
φs1
"H"
"L"
TR2
φhrs
S'
N
Vout

FIG.22

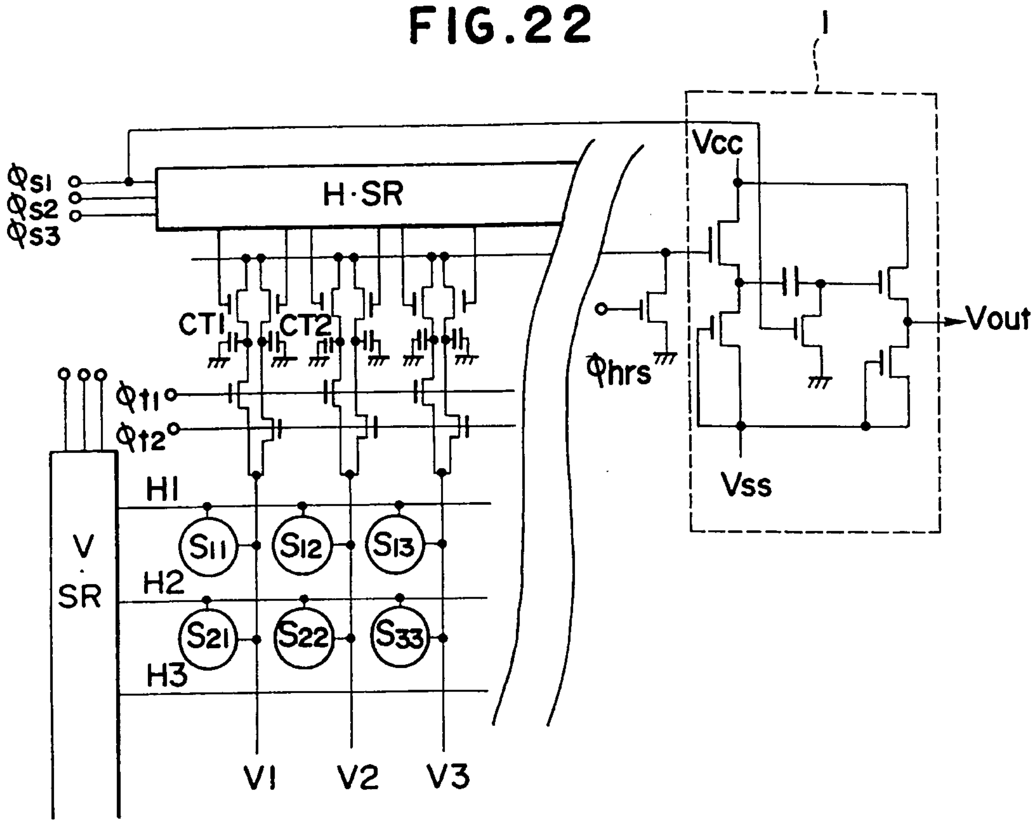
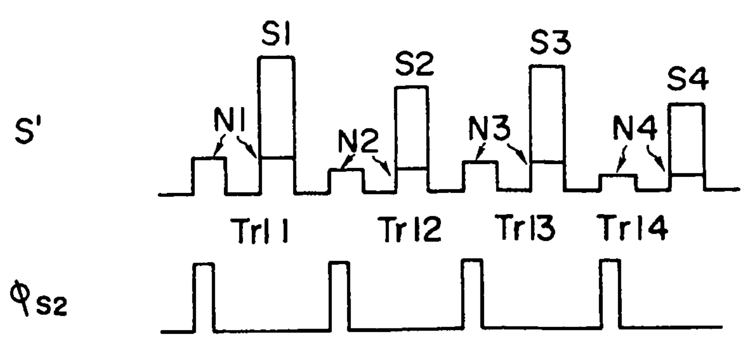

1
Vcc
φs1
φs2
φs3
H·SR
CT1
CT2
φhrs
Vout
φt1
φt2
Vss
H1
V
SR
S11
S12
S13
H2
S21
S22
S33
H3
V1
V2
V3

FIG.23


S1
S2
S3
S4
S'
N1
N2
N3
N4
Tr11
Tr12
Tr13
Tr14
φs2